MICROPROCESSOR BASED RAIL-AXLE COUNTING AND HOTBOX DETECTION SYSTEM

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by

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to the

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JULY, 1982

dedicated to

my parents

CERTIFICATE

Certified that the work entitled 'MICROPROCESSOR BASED RAIL AXLE-COUNTING AND HOTBOX DETECTION' by Dama Venkata Rama R has been carried out under my supervision and has not been submitted elsewhere for the award of a degree.

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ABSTRACT

Hotbox detection and signalling are two important aspects that Railways are very much concerned about. Improved techniques for this purpose are called for because of the need to increase the traffic and speed. Microprocessor based Rail axle counting and hotbox detection system is one such system incorporating advanced techniques with built in safety against human error. The thesis contains the software for a Motorola 6800 microprocessor based system around which the axle counting and hotbox detection system is proposed. The software is developed and tested successfully by simulating real time signals using a toytrain.

CONTENTS

CHAPTER 1

INTRODUCTION

Railways, being an essential part of infrastructure constitute the nerve centre of our economy bearing a lot of strain. What with increasing prices and fast depleting sources of crude oil coupled with abundant national reserves of coal and seemingly exponential growth in population, it is imperative that the strain should multiply. But it has to be borne; borne with increased efficiency and perfect safety. However, it is disturbing that oflate railway accidents have become common place and most often these are traced to signal failures. Lest the economic growth and human life would be in peril, improvement in signalling schemes should be immediately attended to. In this age of computers and 'quick thinking' what else other than micro-processors can comfortably step in! All along this has been the motivating factor.

Since the very beginning of railways the basic aim of signalling is, to monitor a prescribed length of track and give an indication about the occupancy of that particular length of track. Another important direction in which railways were and still are concerned is hotbox detection - which occurs when inadequate bearing lubrication or mechanical flaws

cause a significant increase in wheel temperature. As the bearing temperature rises to an abnormally high level, a bearing failure results. Such bearing failures constitute a major cause of car derailment, endangering life, destroying property, resulting in costly delays and maintenance. Continuous studies and changes in implementation are going on regarding these.

Increasing traffic and higher speeds call for improved control and safety. Current trends in the field of microcomputers, especially the development of very cheap, powerful and reliable microprocessors with elaborate support systems, has made the introduction of computer technology into railway signalling and control inevitable.

This thesis titled 'MICROPROCESSOR BASED RAIL AXLE COUNTING AND HOTBOX DETECTION SYSTEM' mainly aims at software development of combined system for signalling through axle counting and hotbox detection system. The software is developed and tested successfully by simulating real time signals using a toy train. The software is developed for Motorola 6800 microprocessor based system.

1.1 OVERVIEW OF THESIS :

CHAPTER 2 :

In this chapter various conventional methods of signalling and hot box detection systems are described. Their merits and demerits are discussed.

CHAPTER 3 :

In this chapter a new scheme that implements signalling through axle counting and its advantages over the conventional signalling schemes are discussed.

CHAPTER 4 :

This chapter describes the details of infrared hotbox detection system.

CHAPTER 5 :

This chapter gives the specifications of the system, how they are proposed to be met and the approach taken in the development of the software. This chapter also gives a proposed layout of the transducers at the track side.

CHAPTER 6 :

This chapter gives detailed description of the developed software.

CHAPTER 7 :

The thesis is concluded with a critical review of the present work and suggestions for future work.

CHAPTER 2

CONVENTIONAL SIGNALLING SCHEMES AND HOTBOX DETECTION SYSTEMS

In this chapter, various conventional signalling schemes, their principles of operation, merits and demerits are discussed. First various signalling methods are discussed later hotbox detection system is discussed.

2.1 CONVENTIONAL SIGNALLING SCHEMES

2.1.1 Track Circuit - Noncoded DC

The track circuit is the most important link in most signalling systems. It is the vital connection between the train and the rest of the signal system. The track circuit enables us to know just where a train is in a given section of the track. But most important of all the track circuit enables us to provide maximum protection for train movements. ugh the track circuit we can indicate the following :

1. The block is occupied
2. There is no broken rail
3. It is safe to proceed at authorized speed

Track is made of sections and each section is insulated the other section by wax-coated hard vulcanised fibre. In [3] Fig. 2.1.1a track circuit is shown with a neutral track relay,

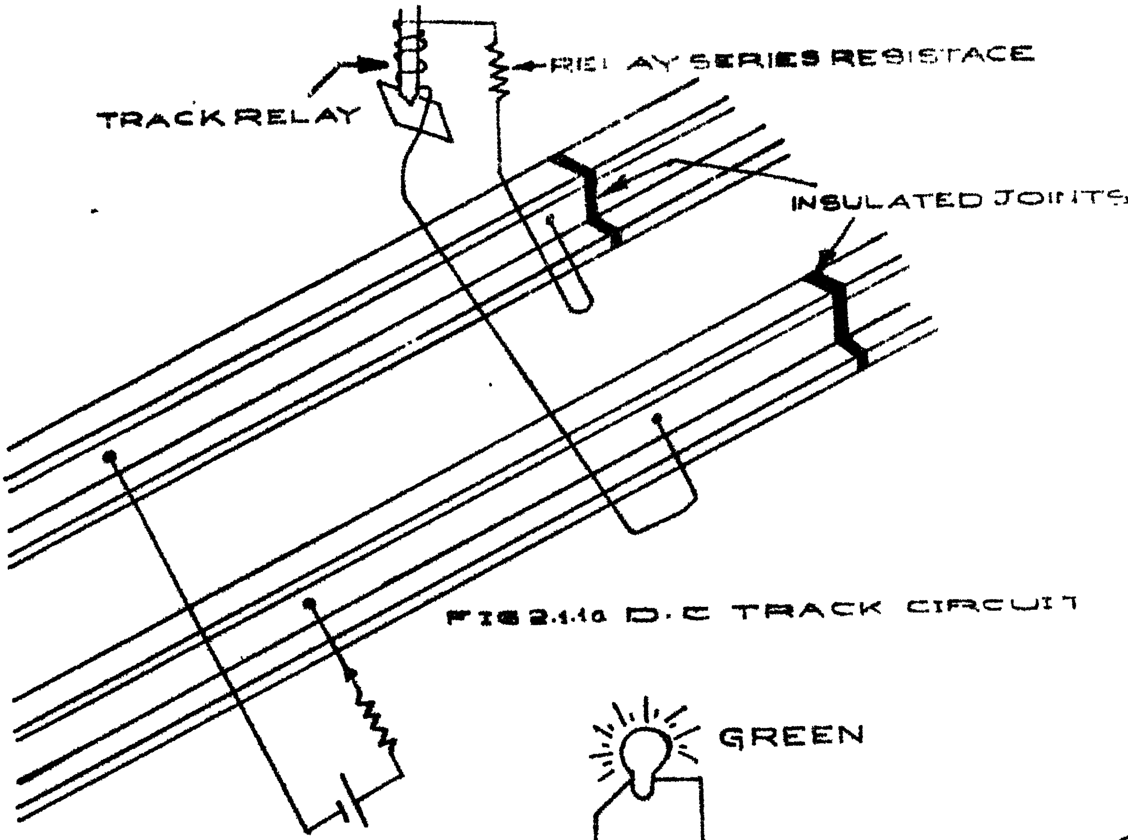


FIG 2.1.1a D.C TRACK CIRCUIT

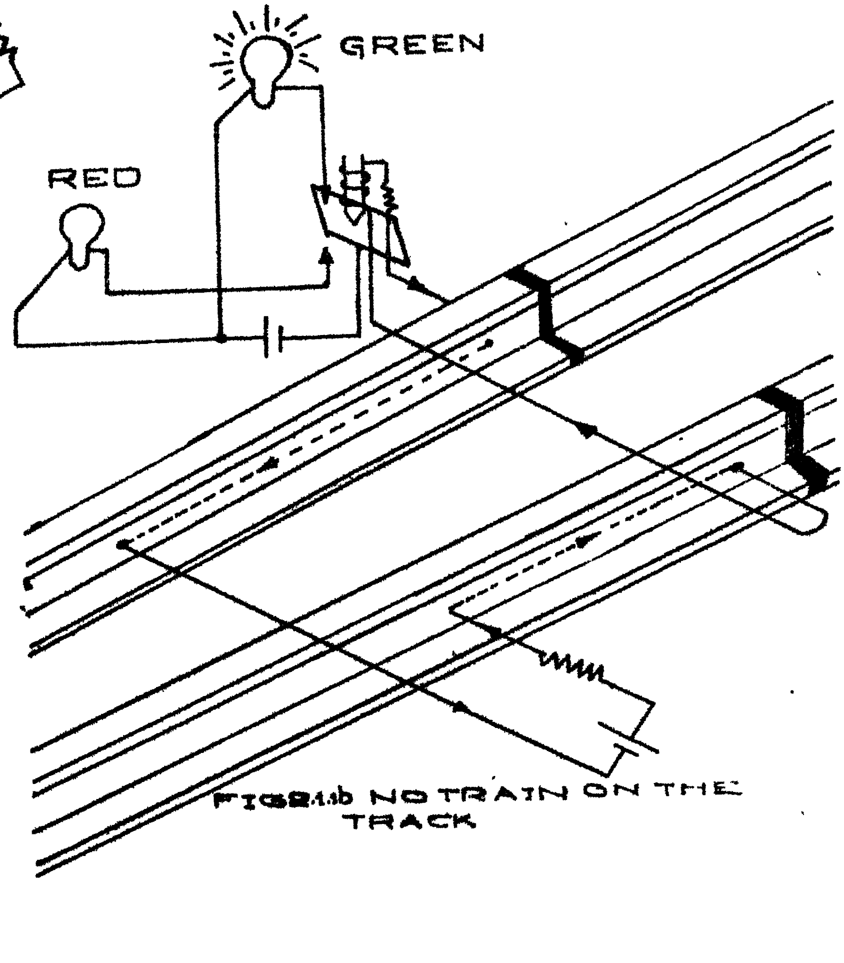


FIG 2.1.1b NO TRAIN ON THE TRACK

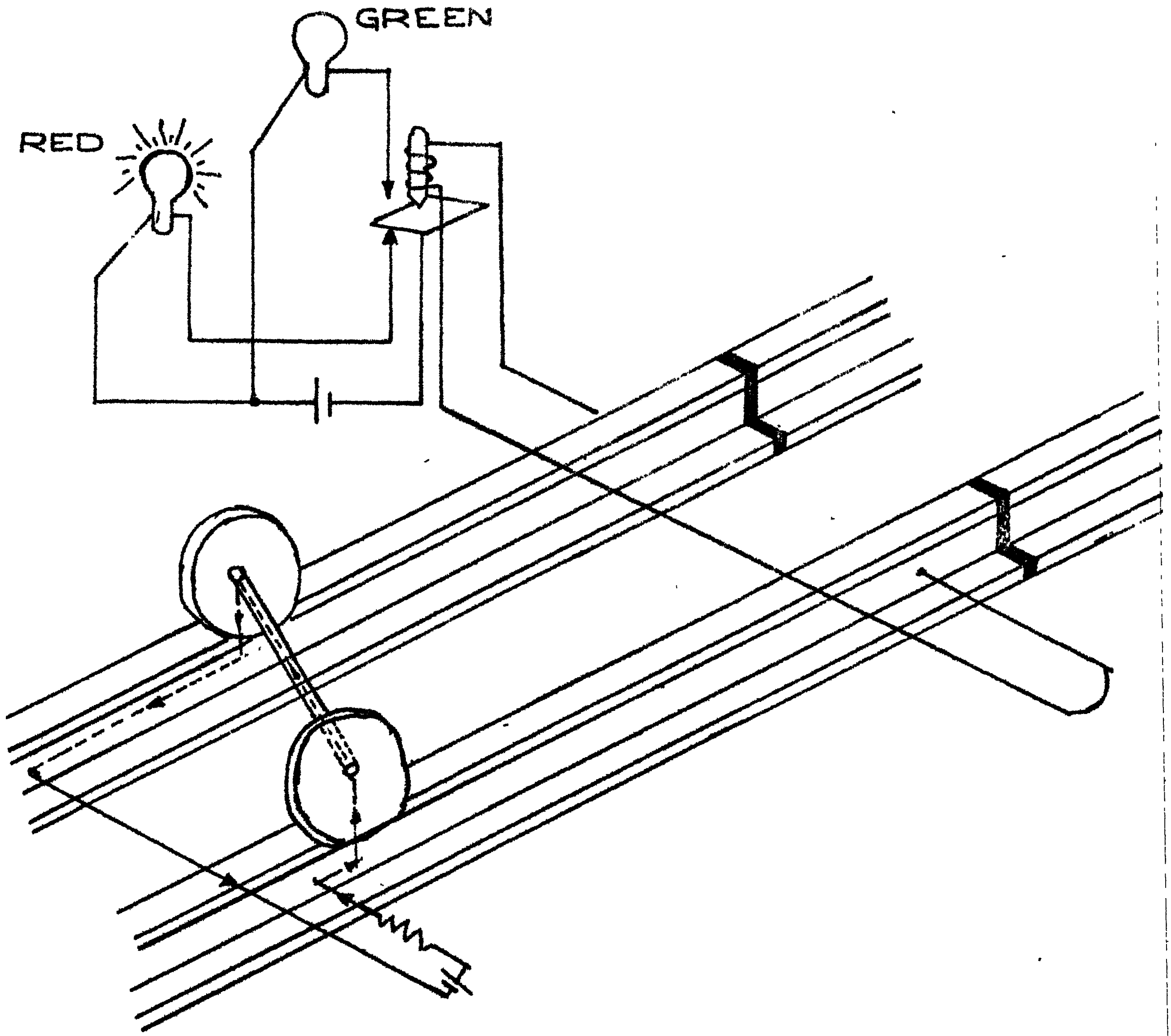


FIG.2.1.1c TRACK IS OCCUPIED (DC TRACK CKT)

which will be energised when sufficient current flows through its coils, regardless of the direction of current flow or polarity of the circuit.

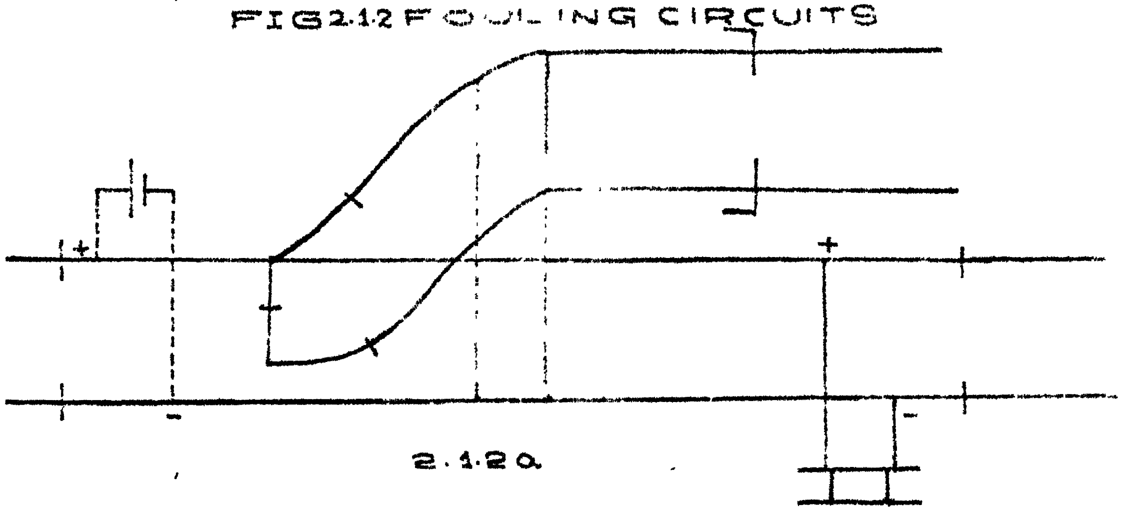
The track circuit operation can be understood from [4] Figs. 2.1.1b and 2.1.1c. Figure 2.1.1b shows the direction of current flow when there is no train on the track section, which energizes the relay, green light is glown, indicating that the track section is CLEAR. When train enters into the track section (Fig. 2.1.1c) it shunts the track relay. With this effect relay is released allowing red light to glow, indicating occupancy of the track section.

2.1.1.1 Crossover (Fouling) Connections Using Noncoded DC Track Circuit

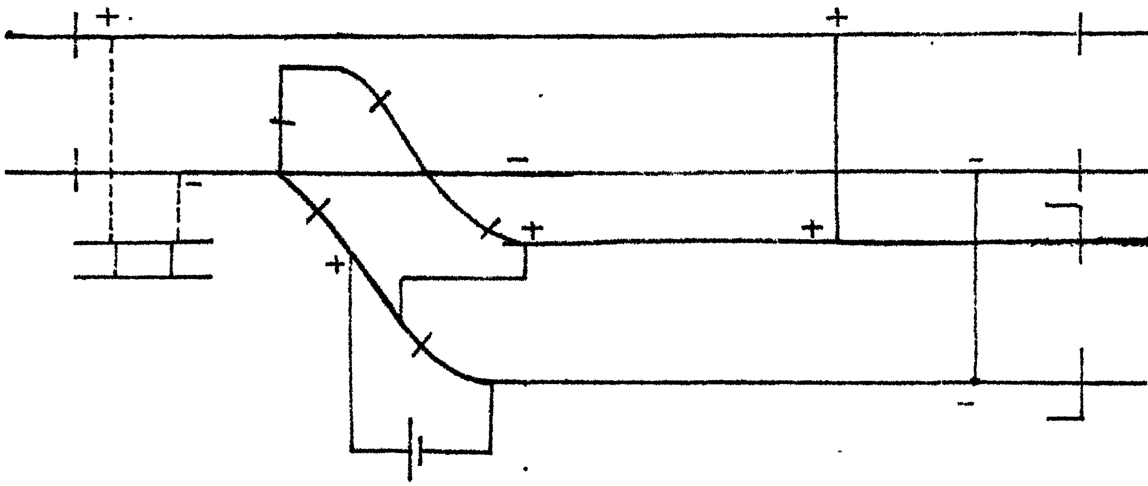
Since the track circuit is used to detect trains within its limits, it must also detect the presence of trains or cars that are too close to permit safe passage. This is done by extending the track circuit limits to the points of fouling along the track circuit.

Figure 2.1.2a illustrates one type of fouling circuit used. That portion of the turnout, within which a car will foul the main line, is connected to track circuit in multiple. The presence of a car on this fouling section will shunt the track relay. When this type of circuit is used, it is essential that the fouling connectors are maintained in good

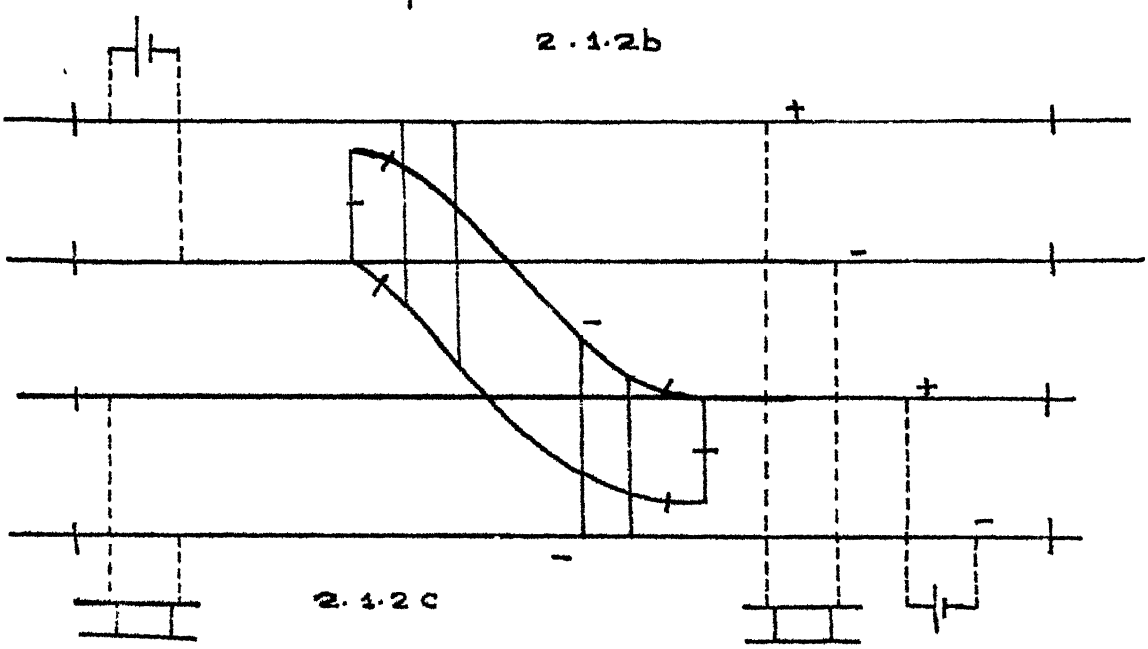
FIG 2.1.2 FOULING CIRCUITS



2.1.2a



2.1.2b



2.1.2c

condition. Breakage of these connectors will result in loss of shunt protection on the fouling section of turn out.

Figure 2.1.2b illustrates another type of fouling circuit used. The fouling section of the turn out is connected in series with the track circuit. This circuit has the advantage of better protection in case of any breakage of fouling connector or a rail as the track circuit will be opened and the track relay will be de-energised.

Figure 2.1.2c illustrates a method used to provide fouling protection on crossovers. The fouling connectors are located so as to connect the fouling sections in multiple with the main track similar to a turn out. The fouling protection on the upper track extends to the insulated joints in the center, as does the fouling protection on the lower track.

2.1.1.2 Considerations to be taken for Installations of DC Track Circuits

'Ballast leakage' is an ever-present factor, which causes a reduction in flow of current to the track relay. It refers to that part of the track current that flows or [5] leaks from one rail to another through the ties, ballast and ground. It is desirable that the ballast resistance to be maintained as high as possible. Fig. 2.1.3a gives simplified drawing of track circuit, the battery, the limiting resistance, the rails, the insulated joints and the relay. Actually the

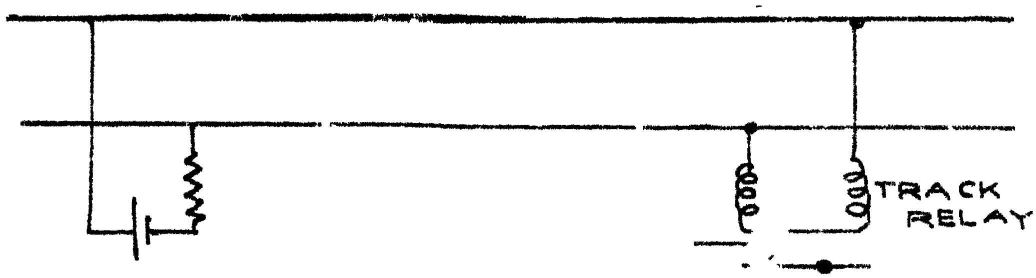


FIG. 2.1.3a D C. TRACK CIRCUIT

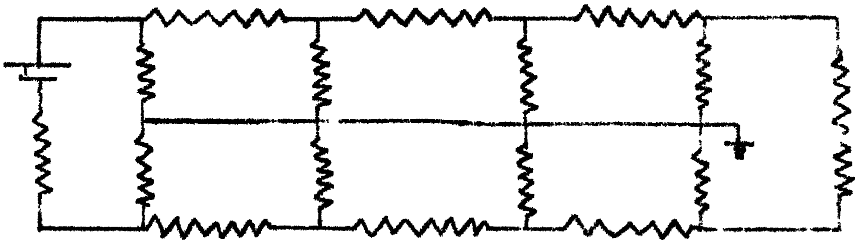


FIG. 2.1.3b BALLAST RESISTANCES

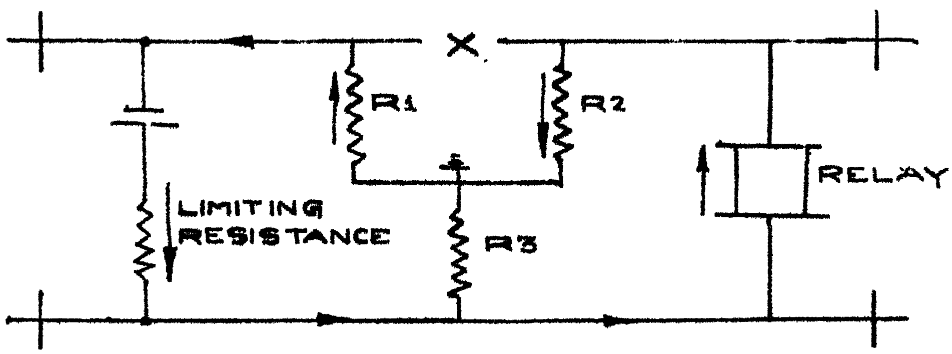


FIG.2.1.3c BALLAST RESISTANCES
(BROKEN - RAIL)

circuit is a network of resistances as shown in Fig. 2.1.3b, the limiting resistor at the battery, the resistance of the rails, the resistance of the relay and the resistance between the rails which is sum of the resistances of each rail to ground.

All this must be taken into consideration when adjusting a track circuit. Bonded rail resistance ordinarily varies from 15 thousandth to 4 hundredths (0.015 to 0.04) ohms per 1,000 ft of track. Ballast resistance may vary from less than one to hundreds of ohms per 1,000 ft of track. In wet weather, ballast resistance usually lessens. In dry or freezing weather it increases.

A ballast resistance network with a rail broken is shown in Fig. 2.1.3c. R1 is the leakage resistance from the battery side of the broken rail to the ground. R2 is the leakage resistance from the relay side of the broken rail to the ground. R3 is the leakage resistance from the opposite rail to the ground.

It will be seen that there are two paths for current from the battery. One is through the limiting resistance and leakage resistances R3 and R1. The other is through the limiting resistance, the relay and leakage resistances R2 and R1. As ballast resistance varies, there may be a relatively critical range of ballast resistance where sufficient current

may flow through the path including the relay to cause improper operation of the relay if the circuit is not properly proportioned or adjusted.

The following are the disadvantages of DC track circuits.

1. When a train longer than the track circuit comes on the track, track circuit will give release when the forward wheels clear the track circuit, and before the rear wheels enter the circuit. The obvious solution is the lengthening of the track circuits themselves but this merely exchanges the problems rather than solving them. Firstly, the cost of lengthening all of the track circuits in a hump yard is prohibitive and in addition, it will defeat our attempts to handle a greater volume of traffic. Thus, the requirements for higher traffic handling are best met by short track circuits while the requirements for handling long cars are the exact opposite.

2. The presence of oil and grease is making the track circuit with light boxer cars distinctly marginal.

2.1.2 Loop Track Circuits

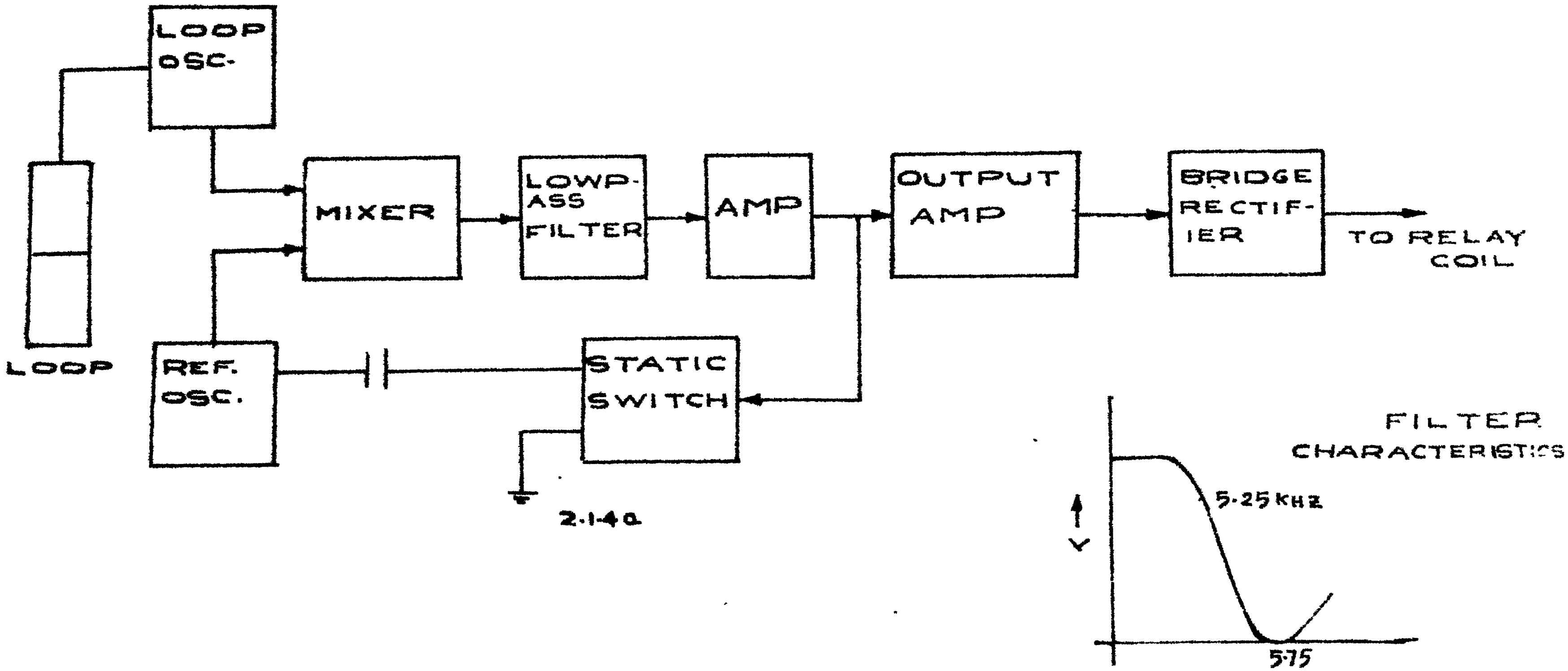
The disadvantages connected with DC track circuit as mentioned above led the loop track circuits to be in use. The [1] design requirements of the loop track circuits are as follows :

1. It should see a car immediately as it enters the area of the loop surrounding the switch, irrespective of the direction or speed of travel.

2. It should continue to see this car until it had cleared the loop completely.
3. If the car stops over the loop it should continue to see it for an indefinite period.
4. Its method of operation must be fail safe in that a failure of any of the components would automatically drop the relay to a locked position .
5. It must not be sensitive to the normal changes of climate to which it will be subjected in a yard, i.e., variations of temperature and humidity and the presence of snow, water or ice.
6. It should have no moving parts, maintenance should be an absolute minimum and the adjustment should require no special skills beyond those normally possessed by a signal technician and with equipment which he would normally be expected to possesses.

2.1.2.1 Operation

Briefly, the unit contains two oscillators (Fig. 2.1.4a), one called the loop oscillator and the other the reference oscillator. The loop oscillator is tuned to approximately 94 KHz while the reference oscillator is tuned to approximately 89 KHz. The output of these two oscillators is fed into a mixer which has as its inputs the two oscillator frequencies and gives as its output a frequency which is the difference between



2.1.4a

2.14b

FIG.2.1.4 LOOP TRACK CIRCUIT

them, in this case approximately 5 KHz. This 5 KHz signal is fed through a lowpass filter which has a cut off at approximately 5.25 KHz to a two stage amplifier followed by a push pull output stage. This output signal, still at 5 KHz is rectified in a bridge type rectifier and the DC voltage so developed is utilized to energize the operating relay.

When a car goes over the loop its inductance is reduced and because this loop is part of the tuned circuit of the loop oscillator, frequency rises by an amount which depends on the dimensions of the vehicle but will be of the order of 500 to 2000 Hz for typical box cars. The reference oscillator remains at its original frequency with the result that the difference frequency as seen by the mixer rises from 5 KHz to some higher value, for example, 6 KHz. When the frequency of this difference signal is applied to the lowpass filter, it is no longer passed by this filter, which cutsoff at 5.25 KHz and the output is thereby removed from the relay.

When the boxer leaves the loop, the loop oscillator returns to its original frequency, the difference frequency drops below 5.25 KHz and the filter then once again passes it and the relay is picked up.

The cutoff slope of the lowpass of filter is made as steep as possible so that the action is suitably rapid but it was felt desirable to introduce what might be described as a toggle action to ensure a positive snap to the switching action.

To achieve this, a portion at the output of the amplifier is rectified and the DC voltage is used to hold open a transistor static switch. This switch puts across the reference oscillator an additional capacity when the voltages falls as the increase in frequency pushes over the edge of the slope. The effect of the increasing capacity on the reference oscillator is to lower the frequency of this oscillator at the same movement we are raising the frequency of the loop oscillator and the difference frequency is thereby violently increased and a sharp switching action takes place as soon as the signal through the filter has dropped by 3 dB.

The DC voltage holding up the operating relay is derived from the 5 KHz signal. This signal is made by utilizing the two oscillators and taking the difference frequency between them. Should either oscillator fail, then the difference frequency would become 90 KHz well beyond the filter cutoff and therefore the relay must drop into the safe position. Should any of the amplifying chain along the way develop a defect, this can only result in a reduction of the amplifier gain and this again would remove the voltage to the relay thereby dropping it to a safe position.

A failure of the power supply would also, of course, drop the relay and as a matter of fact, it can be kept in a place, provided the entire chain of operation is in order. A

A failure of the loop caused by mechanical damage would, of course, disconnect the inductance of the loop oscillator.

The following are the disadvantage of this scheme :

1. Existence of insulated joints, which needs continuous supervision and maintenance of these joints.

2.1.3 Shunt Overlay Track Circuit

Shunt overlay track circuit operates without interference from other track signals and does not require insulated joints and is also failsafe.

In its simplest form, the shunt overlay track circuit consists of a section of track with transmitter connected to one end of the track section and a receiver and relay [2] connected at the other end (Fig. 2.1.5a). It functions very much like the DC track circuit except that the battery is replaced by a transmitter. The receiver consists of an amplifier rectifier and filter in addition to the track relay. Like the DC track circuit, the track relay remains energised as long as the receiver finds a signal (above a certain level) on the track. The presence of a train in the track section will be detected by virtue of the electrical shunt the train produces across the track.

As in the DC track circuit, the operation of the shunt overlay track circuit is hampered by ballast resistance and

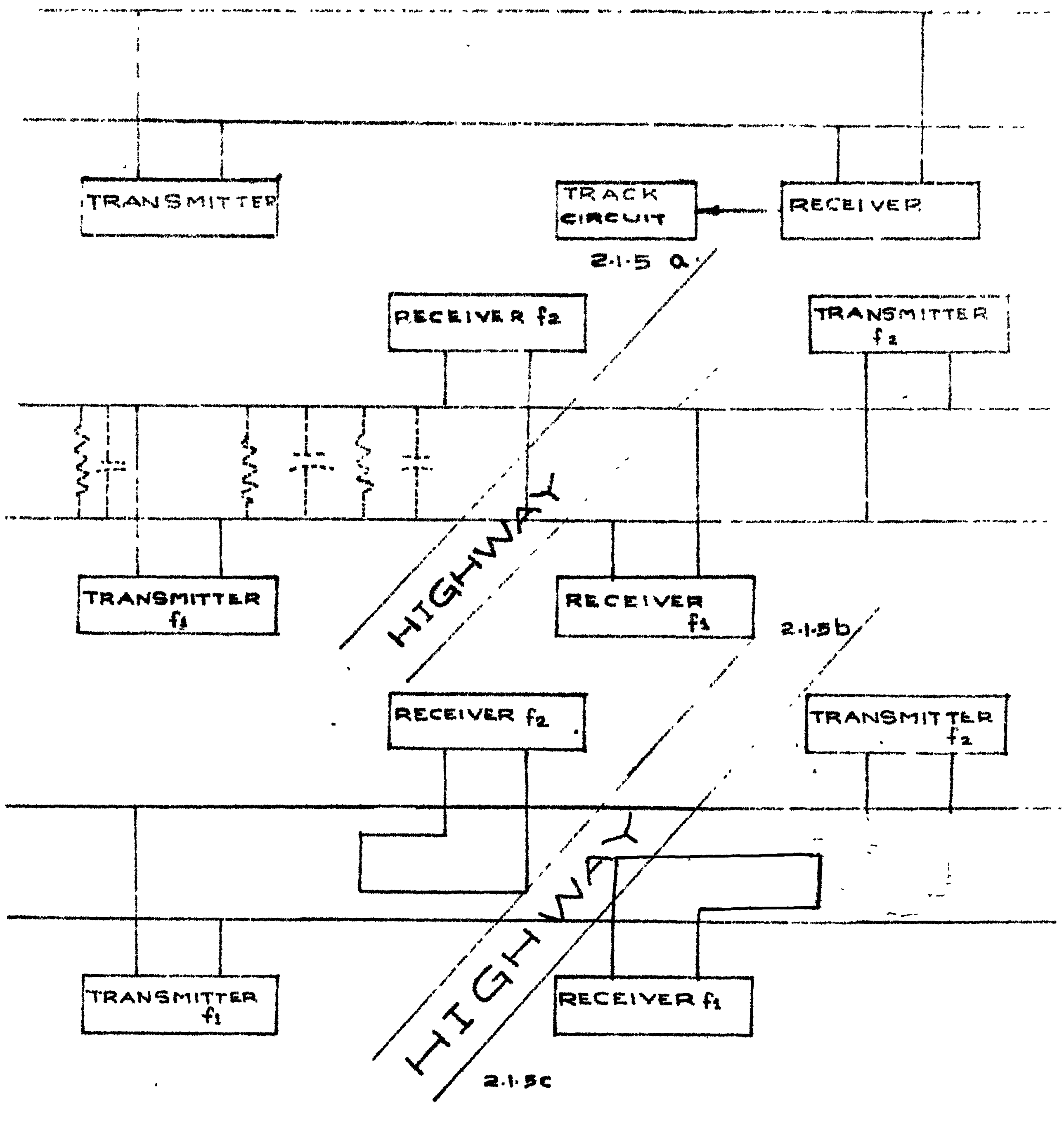


FIG 2.1.6 HIGHWAY CROSSING

the changes in that resistance. For proper operation, the receiver must be capable of 'hearing' the transmitter in the absence of a train and with the ballast resistance low. Yet the receiver must not be able to 'hear' the transmitter in the presence of a train and with the ballast resistance high. Inter-rail capacitance effects are relatively negligible upto a transmitter frequency of about 5 KHz. Most ballasts will run (at its lowest) 5 ohms per 1,000 ft or better. Shunting resistance of a train is generally accepted to be less than 0.06 ohms. Under these conditions, a shunt overlay circuit can be made to operate over 4,000 ft. without difficulty. It is possible to make longer track circuits under somewhat ideal conditions, say upto 10,000 ft. but safe operation is no longer assumed.

In Fig.2.1.5b is shown a single section of track arranged for double direction running with a highway crossing and two overlay track circuits arranged so that they overlap at the crossing. A train shunting the track between transmitter f1 and receiver f2 will indicate track occupancy in receiver f1 but not in receiver f2 : a train shunting the track between receiver f2 and receiver f1 will indicate track occupancy in both receivers; and a train shunting the track between receiver f1 and transmitter f2 will indicate track occupancy in receiver f2 but not in receiver f1.

When a train approaching the crossing from the direction of transmitter f1 it will activate the crossing flashers as soon as track circuit is occupied between transmitter f1 and receiver f1. This same circuitry will keep the flashers operating until the train passes over the crossing and clears receiver f1. Fig.2.1.5b shows symbolically the ballast resistance and internal capacity.

One of the objections to overlay track circuits that is frequently raised is that they do not have a sharply defined 'clear-out' as compared to DC track circuits. After train has passed the receiver and is receding, it still provides a fairly good shunt of the interrail voltage even though the receiver is between the transmitter and the train. How effective a shunt the train provides depends upon ballast resistance. For this reason the 'clear-out' point will vary from about 2 to 75 ft beyond the point of connection of the receiver, depending upon ballast resistance.

If greater resolution than this is required, the receiver may be coupled to the track by virtue of a loop as shown in Fig.2.1.5c. These loops are each 50 ft in length and approximately the width of the track guage. The loops couple the rail current to the receiver. In the absence of a train, rail current is coupled to the receiver and keeps the track relay energized. When a train enters the track circuit, it

shunts the rail current and track relay indicates 'occupancy'. Now, however, after the train passes the loop and is receding, it provides an excellent shunt beyond the receiver loop, causing a heavy flow of rail current and the receiver re-operates its associated track relay. The 'clear-out' point of loop-coupled receiver will vary with ballast resistance from the centre of loop to the end, that is from 0 to 25 ft.

The following are the drawbacks :

1. Loop is costlier to install and maintain.
2. When ballast resistance is unusually high, insufficient rail current will flow, thus the receiver gets insufficient signal to keep the track relay operated. This can be corrected by placing tuned shunts across the track as shown symbolically by dotted lines in Fig. 2.1.5b. These are fail safe since their loss will cause an 'occupancy' indication.
3. From the discussion of Fig.2.1.5 it becomes obvious that transmitter/receiver pairs must be selective so that the receiver responds only to its own transmitter. Disadvantage is that the interference signals are additive. That is, interference signals which can produce distortion products (that lie within the pass-band of the filter) will result in a filter output which adds to the relay current. Naturally, if there are enough of these distortion products, they will produce unsafe condition by providing track relay current in the absence of a legitimate

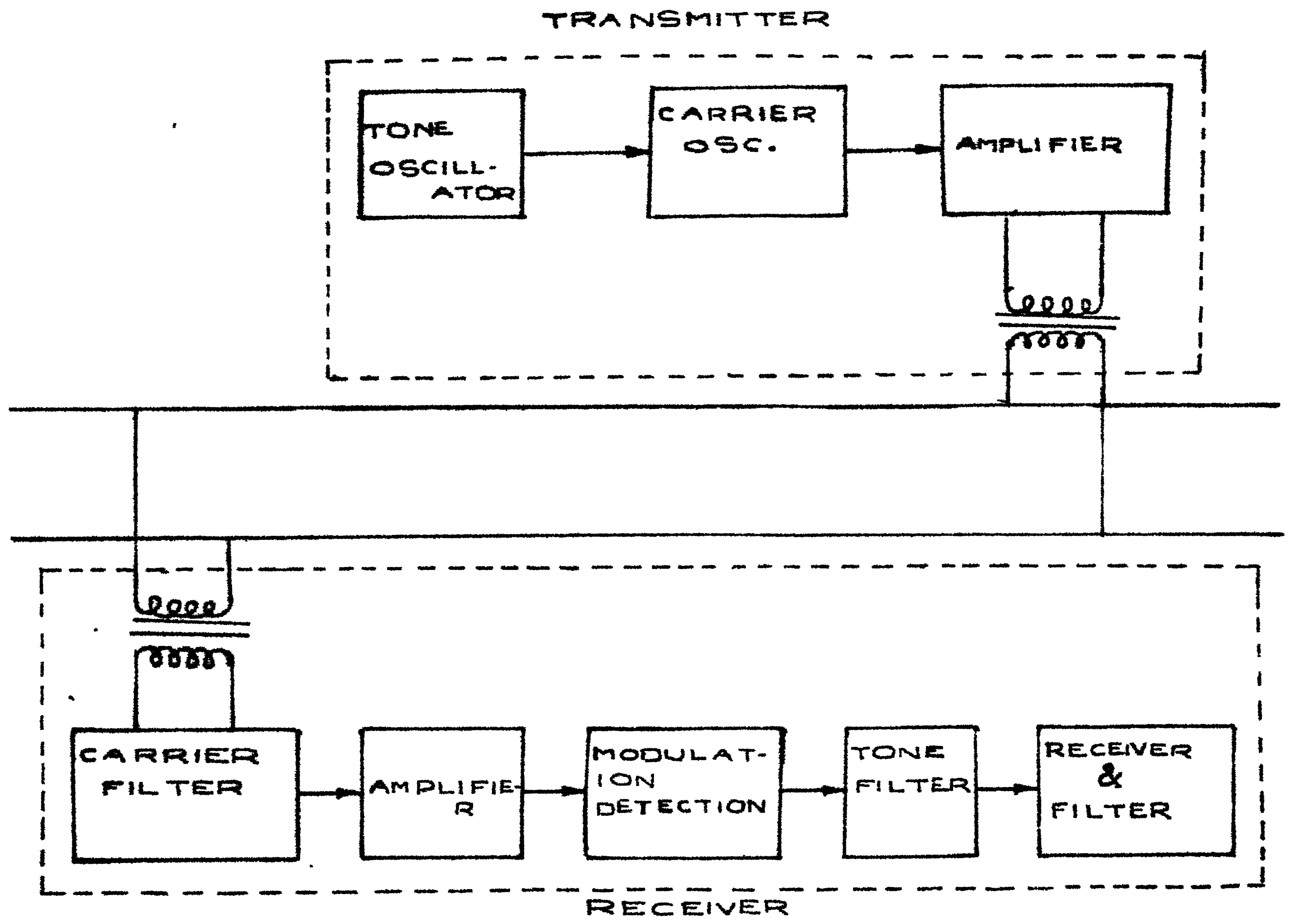


FIG 2.1.6 SHUNT OVERLAY TRACK CIRCUIT

Reduction of interference explained above is possible through the use of tone modulation of the transmitter carrier. Fig.2.1.6 shows a block diagram of such a transmitter and receiver.

The basic difference between the system of Fig.2.1.6 and that previously described is that the track relay is operated from the modulation signal not from the carrier. Thus interference signals, which tends to fill in the modulation, reduce the available output signal rather than enhance it.

The designer must follow the following guidelines in the choice of carrier and modulation frequencies in order to further protect the system.

1. Use non-harmonically related carrier frequencies.
2. Use non-harmonically related tone frequencies.
3. Use tone and carrier frequencies that are not close to or harmonically related to cab signalling, propulsion or public utility frequencies.

2.2 HOTBOX DETECTION SYSTEMS

2.2.1 General Information

Any bearing which departs markedly from the operating characteristics of other bearings in its class on a given train is a hotbox and remedial measures must be taken. [6],[7] In general, the cause for hotbox is the breakdown of lubrication.

The rate of journal temperature variation depends upon the nature of the defect, the loading, the speed of the train etc. One can seldom pinpoint where a hotbox had its origin or how long it will run in an overheated condition before burn-off conditions prevail.

Because an overheated bearing can take one of many paths to the critical stages of destruction, time becomes the most important parameter in the detection process. The journal being obscured from view in its enclosure, can only give evidence of its condition indirectly. For the thermal flux to heat the external box surfaces, the thermal impedance of the assembly (brass, wedge and box) must be overcome. The expression for the thermal circuit of the journal assembly may be given by $T = \varphi \times R$ where T is the temperature difference between the heat producing surface, and the external surfaces of the housing; φ is the thermal flux and R the resistance or impedance offered to the flow of heat.

For all practical purposes the statement serves to point out that the temperature difference between the bearing surface temperature and outside box temperature can be very high depending upon the value of R, Tthe thermal impedance. The value of R depends broadly on the conductivity and mass of the material carrying the heat-flux, if the mass is large and conductivity is poor, a large temperature difference exists, and a large time is required for external surface to reach a

given temperature. It is obvious, that the temperature of the outside box surface is a function of time if a journal box is in the process of overheating.

A normal bearing will achieve an equil ibrium,a steady state temperature,after several hours of running. That is, a heat balance will be obtained and the running temperature will be stabilized. The heat being generated will be exactly balanced by the heat loss of the system. Consequently, the temperature can rise no further unless a defect causes more heat to be generated. If the defect is so severe as to cause the generation of so much heat that the temperature equillibirum point lies above the destruction temperature of the bearing burn-off condition will obtain and unless detected in time, a derailment accident is certain. The difference between normal bearing and the hotbox is that the normal bearing is in a steady-state condition and hotbox is in what is known as a transient condition.

Investigations have shown that the mean temperature for a large number of normal bearings (solid type) is 130°F above ambient temperature. The individual journal temperature will be in a band from 110°F to 150°F, above ambient. These slight variances from the mean temperature are caused by a wide variety of conditions such as, loading, bearing size, bearing contact surfaces, clearances, etc.

The investigations indicated that the normal box mean temperature on the vertical surfaces is about 30^{o}F above ambient. This indicates that above 100^{o}F exists between bearing and outer surfaces of the journal assembly under steady state conditions. Most of this temperature drop exists at the interfaces between the brass and wedges, and the wedges and the top of the box.

About fifteen minutes must elapse between the time that a change takes place at the journal-bearing interface and the time that the box surfaces begin to respond to change. Before a significant detectable change takes place at the hotbox surface atleast half an hour must elapse. The temperature of the journal box cannot give an indication about seriousness of hotbox, because higher indication may have been a hotbox that has been developing slowly and running for hours at elevated temperatures. That box with the lower indication may have had a severe defect causing the journal temperature to rise rapidly but not having sufficient time elapse to heat up external surface before passing over the detector. It remains that it is sufficient to indicate that the box is in a transient condition.

The radiated energy from the target (journal box) is not directly proportional to the temperature in degrees Farenhit, but rather to the fourth power of the absolute temperature.

Another factor which can influence the energy radiated from the journal box is emissivity. It is fortunate that most boxes exhibit like characteristics in radiating energy. Occasionally a box may be newly painted or be covered with cement dust. These conditions would change the surface properties of the journal. Because of these few uncontrolled variables, a temperature measurement is a difficult process. It is a qualitative rather than quantitative analysis that hotbox detector system performs.

2.2.2 Hotbox Transducers

In the past, the manifestations of an overheated bearings were readily indicated by sight (smoke or flame), sound (screeching)or smell (unmistakable odor). Personnel stationed at frequent intervals along the right of way were able to recognise these signs often enough to prevent serious derailments.

With the advent of more efficient technology, hotboxes are detected with the help of what is known as infrared hotbox detector. An infrared hotbox detector is a device which is concerned with infrared energy emitted by the journal box. It is essential that the detector be responsive to the particular wavelength of radiation which the journal box emits. To eliminate extraneous heat sources from the detector the view of the scanner will be blocked with a shutter and allow it to open

long enough to see the target. As added insurance the sensor and the optical material should be chosen which responds greatest to the specific type of radiation given off by the target. The wavelength of electromagnetic energy emitted by the target will be approximately 7 to 15 microns. Germanium is used for optical system to respond to the spectral region we are concerned about. Earlier, light or audio alarm was used to indicate that train has produced at least one abnormal indication. The principle of detecting a hotbox with infrared hotbox detector remain unchanged. Detailed description of infrared hotbox detector is given in Chapter 4.

CHAPTER 3

AXLE COUNTING SYSTEM

Axle counting is a recent scheme of signalling that counts in and counts out the axles when train enters and leaves the track section and gives a 'CLEAR' indication when the count equals; otherwise it gives an 'ENGAGED' signal. It is superior to the conventional signalling schemes described in Chapter 2, because of the following reasons :

1. It's performance will not be affected by ballast resistances.
2. It is a noncontact type, so it will not need insulated track sections, which indirectly reduces the need for continuous maintenance and supervision.
3. Since this works on the principle of tone modulation, interference by distortion products is negligible.
4. The presence of oil and grease on the rails, unlike in the case of dc track circuit will not affect the performance of transducers.

In axle counting system, the axles of the train when passing over the transducers modulate the normal 5 KHz signals of the receiver to form a dip. The signals after amplification are fed on the transmission lines to the indoor equipment which

processes and evaluates the received signals. For two detection point axle counting system (normal main track without any crossovers), four amplitude modulated sinewave signals are converted into digital pulses and these pulses are counted in or counted out depending on the condition that these pulses correspond to the train moving into the track section or leaving the track section.

3.1 DETAILS OF THE TRACK TRANSDUCERS

To monitor a track section, the outdoor equipment is provided at two ends of the section. The equipment at each end consists of

1. Two sets of track transducers, each consisting of :
   - a. Transmitter coil in a composite aluminium fibre glass housing
   - b. Receiver coil in a composite aluminium fibre glass housing
   - c. Base clamp fitted on to the bottom flange of rail for mounting the transmitter and receiver housings.
2. Electronic junction equipment consisting of :
   - a. Oscillator, generating 5 KHz signals feeding two transmitter coils of both track transducers connected in series
   - b. Two numbers of receiver amplifiers for amplification of the signals independently received from two receiver coils of track transducers.

The output of the receiver amplifiers is connected to the cables for onward transmission to indoor equipment.

While the transmitter housing is fixed on the base clamp on the outer side of the rail, the receiver housing is fixed on the inner side. Transmitter coils are energized by the common oscillator. The arrangements and shape of transmitter and receiver coils are such that the two magnetic fluxes generated in the vicinity of the rail and these two fluxes traverse receiver coil in opposite directions.

Reluctance of the magnetic path of the two fluxes is different under normal conditions when no wheel passes on the track transducers. One of these two fluxes is quite large compared to the other and the resultant flux induces a voltage in the receiver coil. When the wheel passes over the track transducers the screening effect of the wheel flange causes a reduction of the larger flux to a value nearly equal in magnitude to that of the other. These two fluxes cancel each other and the induced voltage in the receiver coil falls to a low value.

The ratio of these two fluxes can be adjusted with suitable initial adjustment by rotating the transmitter coil inside the housing assembly. This adjustment depends on the profiles of different rail sections in use.

The track transducers are fitted in the staggered position on the rails of the track. Each transducer coil therefore detects signals which are displaced in time. It is only this time staggering of these signals that gives direction of the train.

The track signals received from the receiver coils of the two track transducers fed independently to a two stage tuned amplifier circuit. The tuned frequency is 5 KHz with a 3 dB bandwidth of $\pm$ 250 Hz. Any noise picked up by transducers in receiver area being a low frequency is suppressed in the receiver amplifier and only 5 KHz signal is transmitted through the cable to the indoor equipment. For proper performance, the output impedance of the amplifier should match the cable impedance.

3.2 INDOOR EQUIPMENT

The track signals may be from an outdoor equipment very near to the indoor equipment or as far as 12 km. Hence, attenuator pads are provided to adjust the signal level to the next section. The attenuators are adjusted so that the input level to the next section is 500 mV peak to peak. The high pass filter filters out 50 Hz and its harmonics and passes the desired 5 KHz signal. This signal is amplified, rectified and fed to lowpassfilter which filters out 5 KHz signals and gives the modulating signal representing wheel dips. This

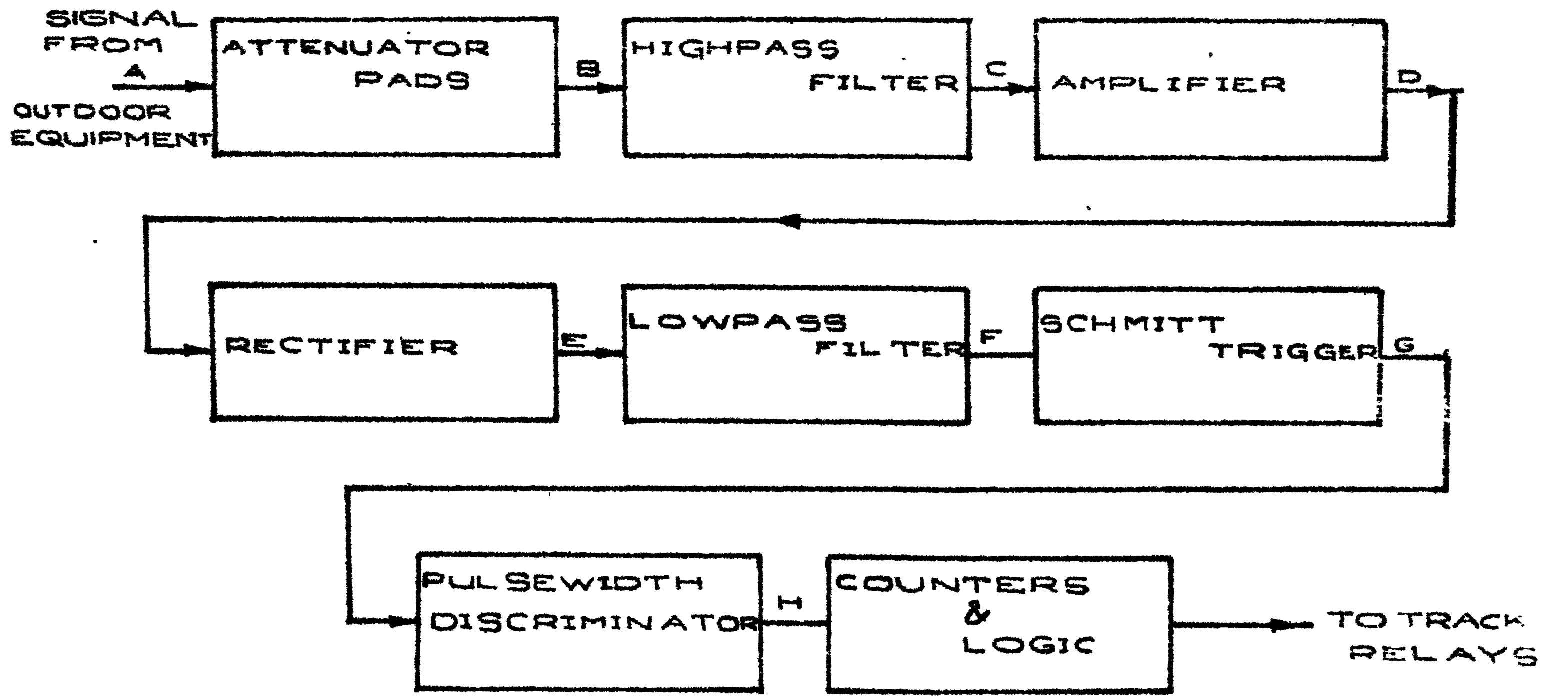


FIG.3.1 INDOOREQUIPMENT

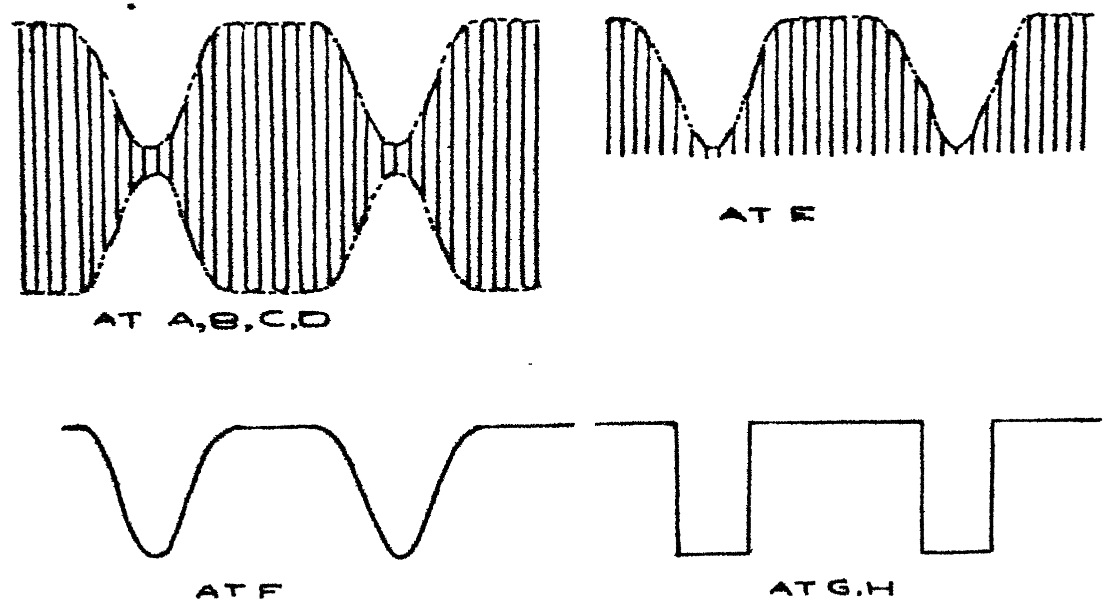


FIG.3.2 WAVEFORMS AT VARIOUS POINTS OF THE INDOOR-EQUIPMENT

demodulated signal is converted into pulses by Schmitt trigger. The pulse width generated by normal train axles is always greater than 7 ms even at a train speeds of 200 kmph. Any pulse less than 5 milliseconds duration therefore represents the noise induced in the system due to extraneous sources. The pulsewidth discriminator cuts out the pulse having a pulse width less than 5 milliseconds and passes other pulses to the counters. For a two detection point axle counting system four similar types of pulses staggered in time are fed to the counters. The counters and logic counts in or counts out the pulses depending on the movement of the train on the track section. Logic involved is explained in Chapter 4 in detail in conjunction with proposed system. The logic will take care of all types of train movements (shunting and through running). Typical waveforms at each input block of Fig. 3.1 is shown in Fig. 3.2. A better signal processing scheme is suggested in Chapter 5.

CHAPTER 4

INFRARED HOTBOX DETECTOR

In this chapter the principle of operation of the infrared hotbox detection system is explained in detail. An infrared hotbox detector is a device which is concerned with infrared energy emitted by the journal box.

In a basic arrangement for a bidirectional system with single junction box, figure 4.1a, or multiple junction boxes, fig. 4.1b, magnetic wheel detectors on both approaches to the scanner location initiate system operation. The track mounted equipment for a single junction box system consists of two mounting assemblies (scanner and blower), four wheel detectors, a junction box, and connecting cables.

A basic unidirectional system does not require wheel detectors 2 and 4, fig .4.1a or 4.1b and a directional relay printed circuit board. An optional reverse direction lockout features may be available to avoid scanning in the reverse direction.

4.1 BASIC OPERATION

A train approaching the scanner location turns on the system when it passes over the advance wheel detector, figs.4.1a or 4.1b. A control pulse generated by the wheel opens the scanner door and starts the pen recorder.

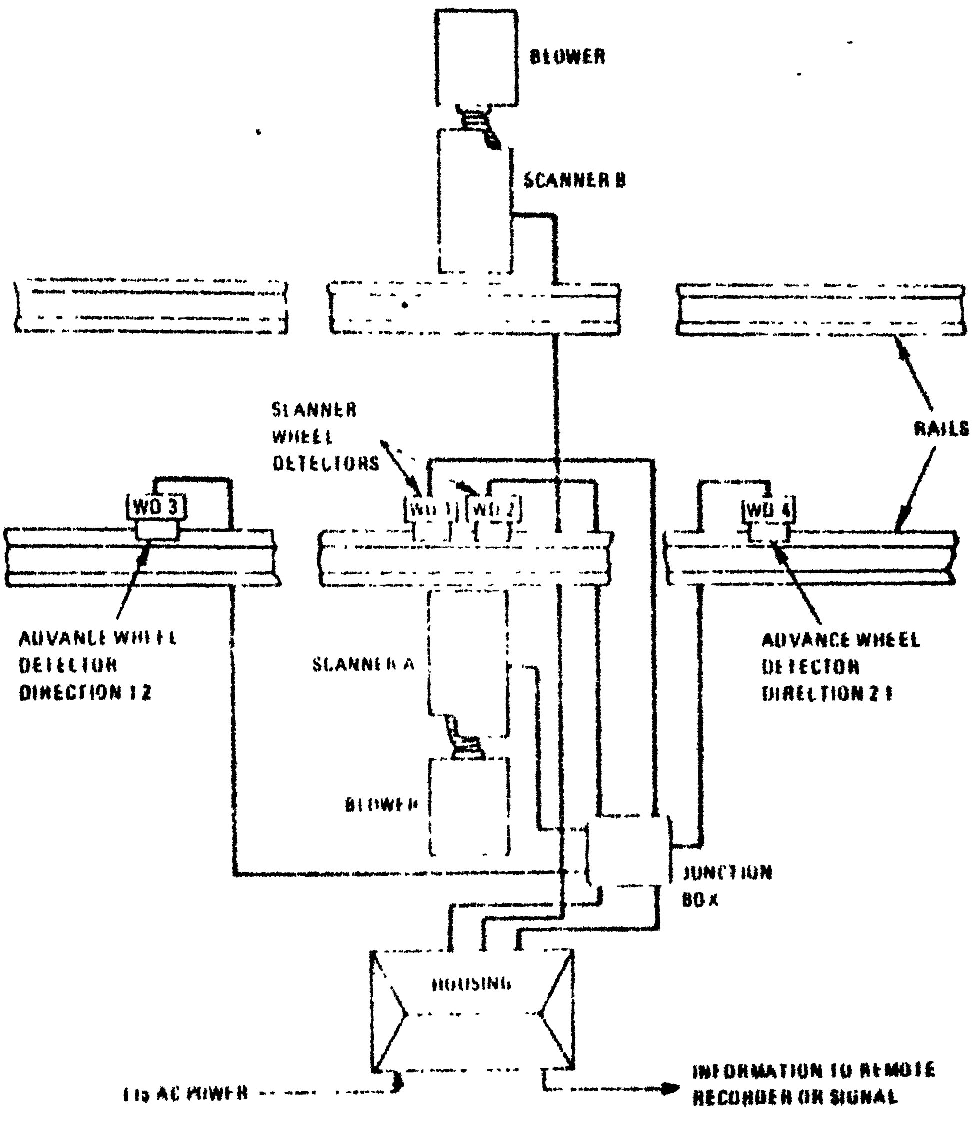


Figure 4-10 Basic arrangement of a bidirectional system - single-junction box arrangement for systems manufactured after 1974.

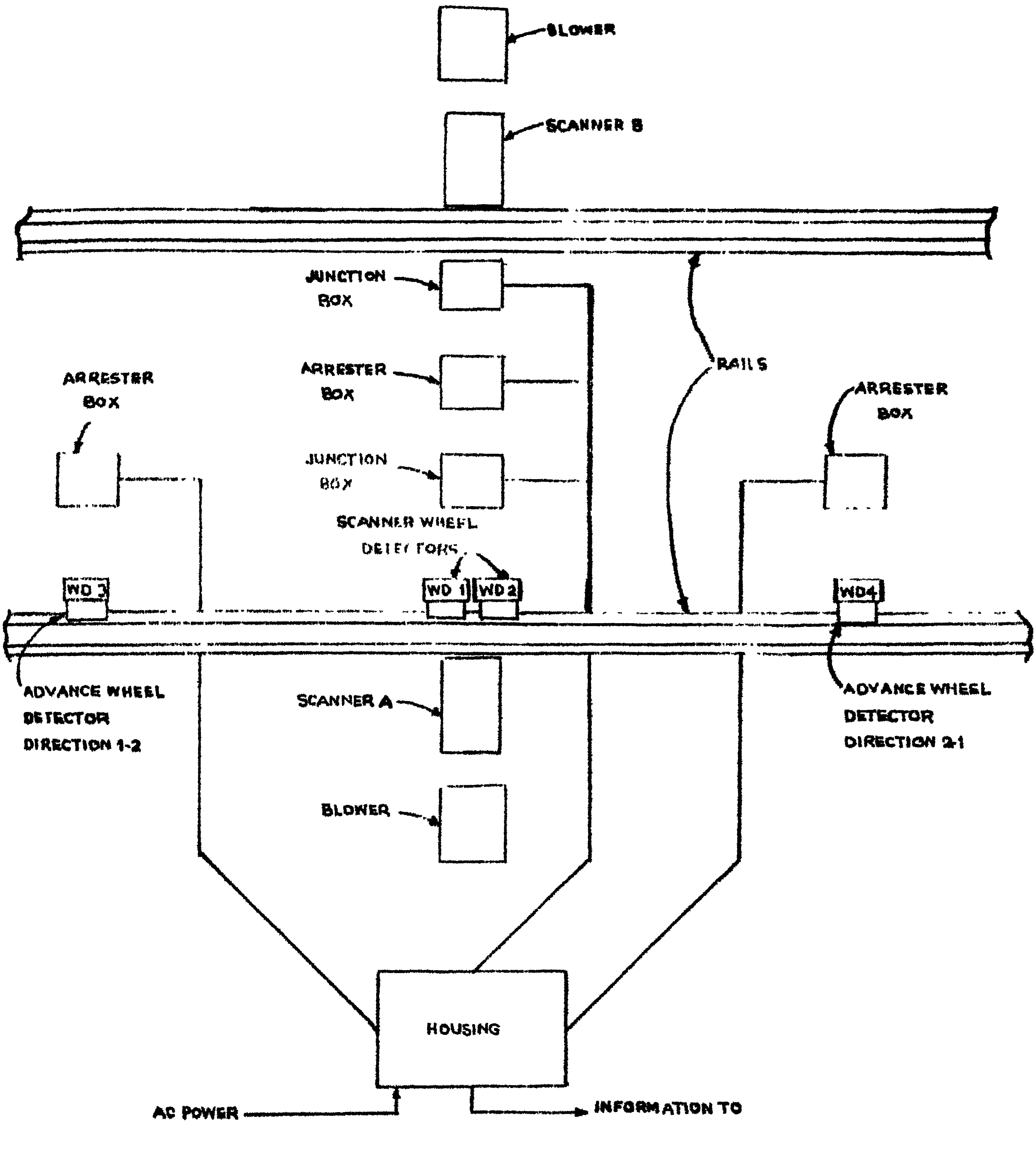


Fig 4.1b. Basic arrangement of a bidirectional system

The passage of each wheel over the scanner wheel detector results in a pulse that is processed by the gate generator and amplifier gate units located in the way side housing. The output ultimately operates the optical shutter in the radiometer (located in the scanner) to briefly expose a small infrared detector. Radiated infrared energy from the passing journal is collected and focussed on the detector which produces a current proportional to the total amount of collected infrared energy. The current is converted to a voltage and amplified in the radiometer. This voltage pulse is fed to the amplifier gate unit to drive pen recorder.

After scanning the last journal, a timing network on the gate generator unit allows 14 seconds to elapse, and then closes the scanner door. About 1.5 seconds later a check pulse causes the radiometer to view a reference target on the inside of the scanner door to determine that the system is functioning properly. The system now reverts to a standby mode during which system sensitivity is automatically checked and adjusted in every minute.

4.2 SCANNER

The radiometer is mounted at an angle in the bottom of the scanner case, Fig. 4.2, so that its window is protected from snow, dirt, etc. A front surface mirror, also mounted in the bottom of the scanner case, is made of chromium-plated brass which is polished on both sides. Should it become

scratched after several years use, it can be turned over. The 2 watt mirror heater is continuously energized from the 24 volt dc supply.

The radiometer is hermetically sealed to prevent the entry of dirt and moisture.

The detector, a one millimeter square metallic crystal, changes its resistance when exposed to infrared radiation - it is photoconductive. A thin layer of vapor deposited metal on the surface of the detector reflects visible light but allows heat to pass.

The detector is accurately located at the focus of a precise system of flat and parabolic front surface mirrors. This optical system focuses a beam of heat from a ½ inch square spot on the wheel hub through the open scanner door to the chrome mirror in the bottom of the scanner case, thence to the parabolic mirror in the radiometer, the flat mirror on the inner side of the radiometer window, and to the infrared detector.

The shutter normally interrupts the beam of heat to prevent undesired stray infrared radiation from striking the detector. The passage of a wheel over the scanner wheel detector generates a gating pulse which rotates the shutter to expose the detector at the precise instant the wheel hub comes into the field view. The shutter is open only a few

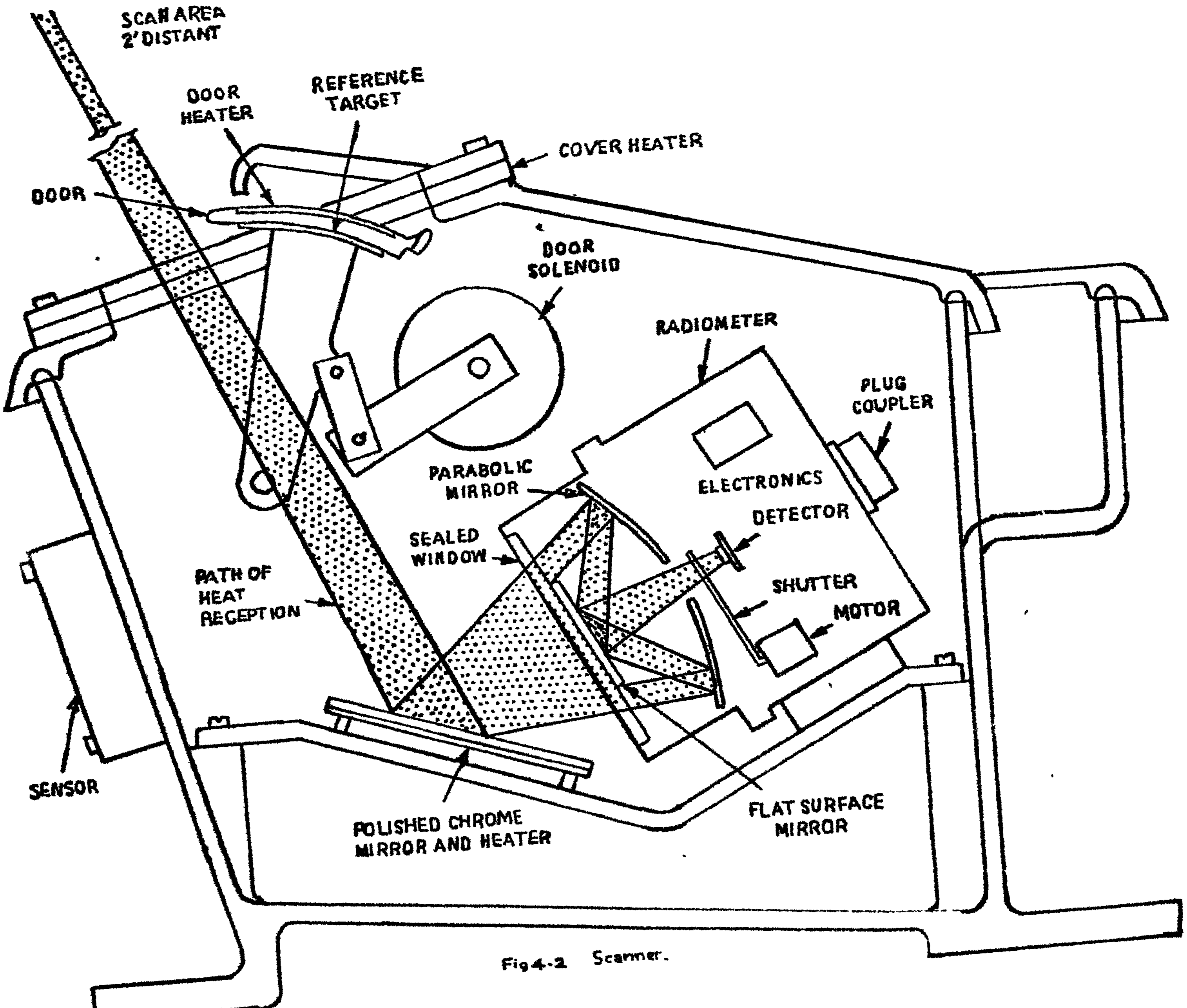


Fig 4-2 Scanner.

milliseconds, thus establishing the length of the heat pulse generated by the detector. The heat pulse is amplified in a high-gain preamplifier, located in the radiometer, and fed to a line driver.

4.2.1 Door and Cover

The door located in the scanner cover, Fig. 4.2, is opened by a rotory solenoid and closed by a spring and counterbalance weight. The solenoid is connected to the door by a dead center mechanism which locks the door to discourage vandalism. The return spring is not effective as the door starts to open, thus the full power of solenoid is able to set the door in motion and fully stretch the spring at the open position. When energy is removed from the solenoid, the spring quickly closes the door. The 20 watts heater on the door melts accumulated snow.

4.2.2 Reference Target and Sensor

The reference target, Fig. 4.2, a heater mounted on the underside of the door, and the sensor, attached to the front of the scanner case, are parts of the systems self calibration feature.

4.2.3 Blower

The blower is equipped with a replaceable type filter, a screen, snow baffles, and a hood. The filter should last for

several months, depending upon environment conditions.

4.2.4 Wheel Detectors

The wheel detector is epoxy encapsulated magnetic device tie-mounted on the inside of the rail about 1/4th inch below the location of the wheel flange. This type of mounting eliminates the need for rail drilling and the problems of rail creepage. The magnetic structure contains permanent magnets which set up a flux field through the coil. When the wheel approaches, Fig. 4.3, the magnetic flux builds up until the wheel is exactly over the centerline of the structure and then decays as the wheel recedes. A current is generated in the coil, the action of this flux current has one polarity during flux build up and the opposite during flux decay.

The point of current reversal is accurate to wheel centre position within $\pm$ 1/4th inch. The coil is protected from lightning damage by the arresters in the main junction box, Fig. 4.1a or by the associated arrester box, Fig. 4.1b.

4.3 OPERATION

As the train approaches the scanner location, it first passes over either advance wheel detector 3 or 4, Fig. 4.1a or Fig. 4.1b. This announces the arrival and will readies the system for operation. It also establishes train direction, which is used to select the scanner wheel detector preceding the centerline of the scanner. For examplé, if advance wheel

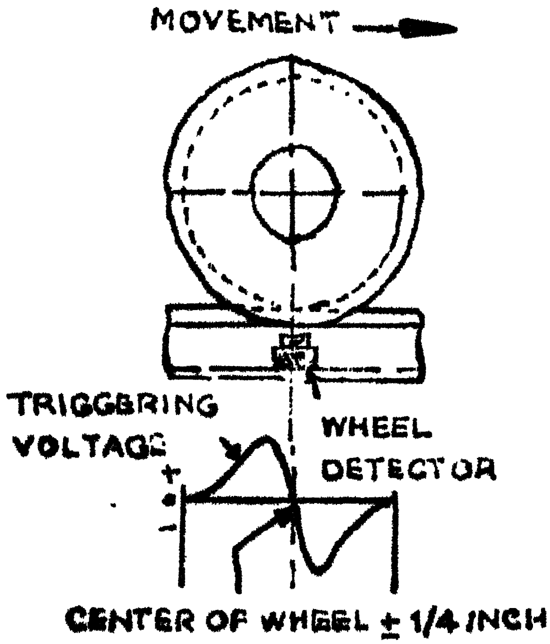


Figure 4.3.
Wheel detector output current.

detector 3 is actuated, scanner wheel detector 1 is selected. This direction is referred to as direction 1-2, with reference to the scanner wheel detectors.

The train next actuates WD1 which causes the scanner to scan the journals and convert radiated heat energy to electricity on a proportional basis. The electrical analog of the wheel heat profile is carried by cable to the housing where electronic equipment extracts the information desired.

The activation of an advance wheel detector and selected scanner wheel detector operates a 14-second timer which keeps the system in operation. When train slows and stops at the scanner installation, the timer times out and the scanner reverts to standby operation. If a track circuit relay contact is available, or if overlay transciever is provided, the direction of train movement is retained. If, however, no track circuit information is available, the train direction is lost. For this reason, track circuits are recommended where trains may stop. When the train starts again, the first wheel over an active wheel detector reactivates the system which continues to scan the remaining wheels until last wheel passes. After 14 seconds, the system again reverts to standby operation, and when the track circuit clears the directional memory is released.

4.3.1 System on Standby

During the absence of a train, the wheel Thermo-Scanner system is on standby. Standby operation involves a self-calibration feature, which once in every minute opens the radiometer shutter. The normal optical path of the radiometer is, however, blocked by the door, which is closed during standby operation. As previously described, the target on the inside of the door is heated to a temperature above ambient which is indicative of an overheated journal (hotbox). Thus the radiometer reads the temperature of the target. In the wayside housing the amplifier gate board analyses the output voltage if it is a level other than expected from a hotbox the gain of its amplifier is changed to bring the output to the proper level. This gain is controlled by 32 step digital counter.

The heavy lines on the block diagram, Fig. 4.4, outline, this operation. Starting with the heavy lined block, the normally running pulser produces pulses once in every minute. The pulses pass through the gate control circuits and open the shutter in the radiometer. With the door closed, the radiometer reads the target temperature which is translated by the preamplifier to a potential of about 1 volt. The heat pulse is fed by the line driver in the scanner back through the cable to the test unit board in the modular equipment cabinet where an electronic circuit clamps the output pulse

after a predetermined time. The clamp circuit terminates the heat pulse about 6 ms following the opening of the shutter. The heat pulse is fed to an amplifier and a peak storage device (a capacitor with isolation circuitry). The device stores the highest voltage attained from the time the shutter is opened until the signal is clamped.

A fixed voltage pulse (called a pedestal) is added to the heat pulse. The pedestal is normally 0.5 volt in height. The combined heat pulse and pedestal is fed through a gate circuit (controlled by the same gate pulse that originated the shutter movement) to the comparator.

The comparator checks that the voltage of the combined pulse (representing a hot journal) is between 1.8 and 2.2 volts. If the voltage is not within these limits, sensing circuits within the comparator step the 32-step stepper one step in the direction required to correct the situation. The 32-step stepper controls the gain of the amplifier through which the heat pulse was fed before the peak storage. When the heat pulse is low, the comparator causes the stepper to increase the gain in the amplifier so that after one or more steps the pulse is of the expected height. This ensures that, during normal operation, heat measured from an overheated journal (at the same temperature as the target) displays a 10 mm pulse. The hot journal threshold.

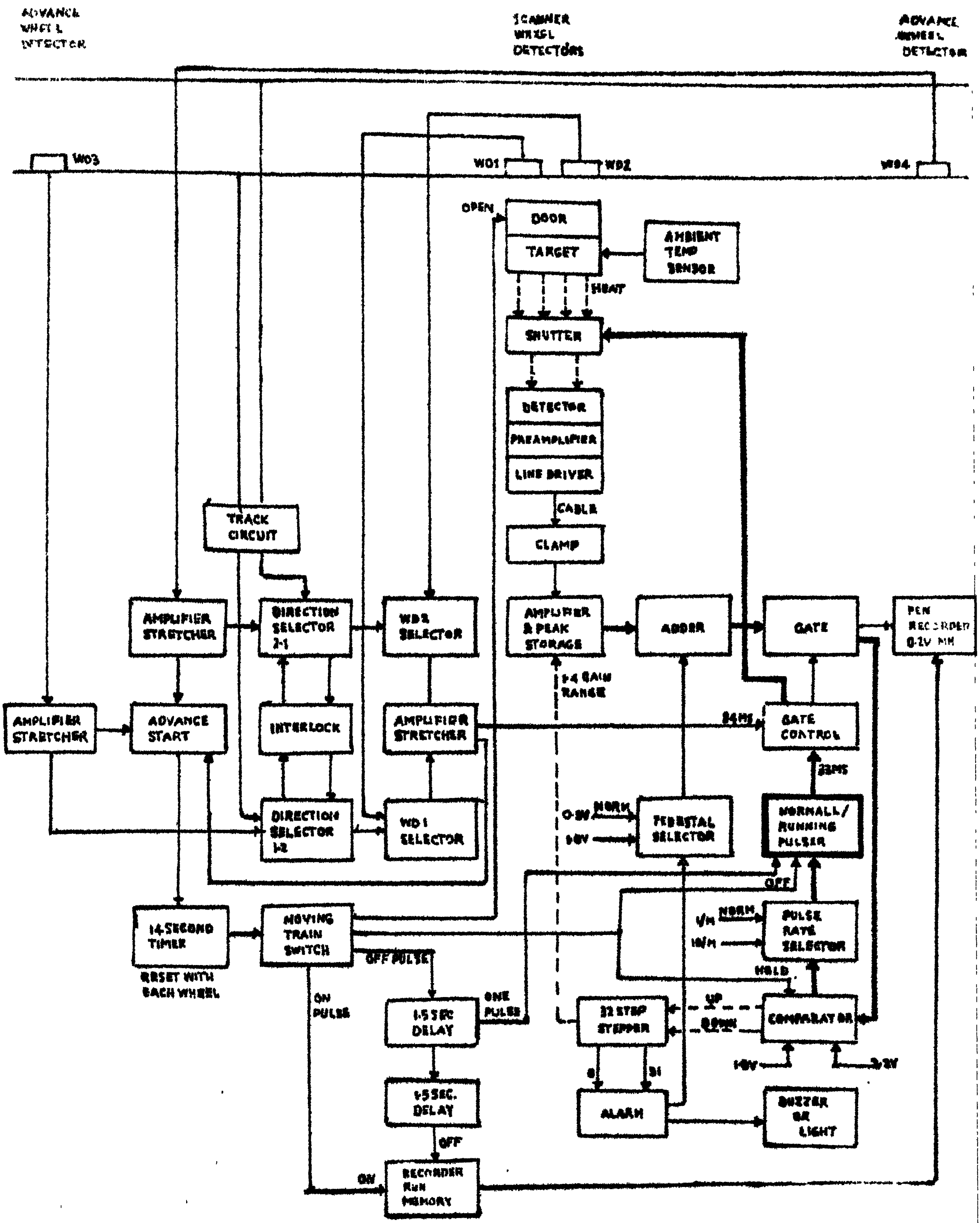


Fig. 4.4. Block diagram, bidirectional system operation.

A supplemental comparator circuit, the pulse rate selection governs the pulse rate of the normally running pulser by increasing the rate from one per minute to ten per minute any time the comparator detects a pulse out of tolerance. This ensures prompt correction of any gain change and is especially valuable during the initial start up and test. Things which might cause a change in the heat pulse output are dirt on the optics, component aging, ambient temperature changes and faulty system alignment.

A second supplemental circuit in the 32-steps stepper is an alarm circuit. It senses when stepper has stepped either to the top or bottom of its range. The circuit then causes the pedestal selection to double the pedestal voltage. This switches on a transistor relay driver (for external alarm) to warn the person reading the tapes that the system is no longer able to compensate for whatever condition is causing the heat pulse reduction. When such a condition is corrected the comparator steps the gain back down again to get the heat pulse within tolerance. The comparator does not operate during normal system operation; just during standby.

4.3.2 Train Approaches

As the train approaches the scanner site, it occupies the track circuit (if one has been provided) so the direction established when the train first actuates the advance wheel

detector is maintained during the trains presence. This may be a spare contact on an existing track relay, if such is available or it can be a series overlay.

The train after occupying the track circuit, passes over the advance wheel detector. The electrical pulse generated by the wheel detector coil is fed over a cable to the wayside housing where it is amplified and shaped by an amplifier - stretcher that picks up an interlocked relay in the direction unit board (the direction selector) to establish the train direction. The relay is held by the track circuit. The activated direction selector selects the proper wheel direction for operating scanner.

The gate generator associated with the advance wheel detector and the selected scanner wheel detector have a second output - to provide an advance start for taking the system out-of standby and readying it for operation. The advance start circuit actuates a 14 second timer which is reset to zero when a wheel passes a wheel detector. The timer in turn operates a moving train relay as long as wheels keep resetting the timer and turns off 14 seconds after the last wheel pulse. While the relay is energized, a pulse is delivered to the recorder run memory which activates pen recorder. A second function of this relay is to open the scanner door, removing the calibration target from the view of the detector. A third function is to stop the normally running pulser and hold the

comparator and therefore, the 32-step stepper position it had attained at the time of the trains arrival.

The distance between the advance wheel detector and the selected scanner wheel detector must be long enough to allow the door to open, before the train reaches the scanner.

When a wheel passes the selected scanner wheel detector, the associated gate generator applies a 24 ms pulse to the gate control circuitry in the same manner as the normally running pulser did during standby operation. The gate control circuitry opens the shutter allowing a detector to view the passing wheel hub, which has in the meantime moved into view. The heat received during the wheel scan is converted into electrical energy in the same manner as described under standby operation. The heat pulse is gated, amplified, stored, stretched, and added to the pen recorder where it is displayed.

4.3.3 Train Leaves

When the last wheel passes over the trailing advance wheel detector, the 14-second timer receives its last pulse. 14-seconds later, the timer turns off the moving train switch which closes the scanner door, thus interposing the calibration target in the detector field of view. The off pulse of the moving train switch starts a second timer which, 1½ seconds later (to give the door time to close) puts a single pulse into the pulser to open the shutter in the usual way. One and a half seconds after

the second timer operates, a third timer operates which turns off the recorder run memory. The action is the same for a train that slows and stops.

Following the scanner shutdown, calibration pulse, and recorders shutdown, the train eventually clears the track circuit. When it does, the directional memory is dropped and the system is ready once more to accept a train from either direction. The system is now in standby and returns to it self-compensating function.

CHAPTER 5

PROPOSED SYSTEM

The proposed system takes care of the signals that come from both hotbox detector and axle counter transducers and gives appropriate indication after processing them. The software that takes care of both functions of hotbox detection and axle counting is developed for M6800 based system and tested by simulating real time signals using a toy train. This chapter gives detailed description of the specifications of the proposed system, how they are proposed to be met and the approach taken in the development of the software.

5.1 SIGNALLING SCHEME

5.1.1 Specifications

The specifications that are typical are given below :

1. The track mounted electronic detection equipment shall be non-contact type and will not infringe the standard moving dimensions. It shall consist of a suitable transmitter and receiver with an electronic junction box. The transmitter is to give an output at 5 KHz ± 15 Hz frequency. It shall electronically sense the passage of wheels and transmit modulated signal at 5 KHz ± 15 Hz and shall be actuated by wheel flanges and not by other parts of the train (rail brakes, toilet pipes, suspended clamps etc) and its operation

shall be independent of

a) the type and condition of the wheels such as diameter, design of wheel, wear and tear permitted,

b) the type of rail section and construction such as welded or non-welded rails and

c) the type of traction such as electronic, diesel or steam and the weight of rolling stock.

2. The information generated by the track detection equipment shall be processed by a microprocessor based system.

3. The equipment shall count in or count out the axles at every end of the nominated track section depending upon the direction of the train.

4. The equipment should be capable of being connected with four detection points simultaneously with one processor.

5. The operation of the equipment shall be fully reliable at all train speeds in the range of '0' to 200 km per hr. The equipment shall ensure that until all the axles that enter a section are completely counted out, the section concerned shall not be shown as clear.

6. The equipment shall be capable of simultaneously counting in and counting out, that is simultaneous counting in and counting out of the pulses from any end shall not interfere with each other.

7. The equipment shall not be susceptible to operation by maintenance tools at or near the track equipment.

8. The equipment shall be insensitive to extraneous magnetic or electrical fields (such as due to traction return currents or electrified traction motor fields, vehicle magnets for induction train control, wheels with residual magnetism etc., or due to any other sources).
9. Detecting equipment at a junction of two consecutive sections shall be able to control seperate processors for each section, i.e., each detection point should be capable of being fed to two systems.

To meet the above mentioned specifications axle counting scheme is chosen because of the advantages mentioned in Chapter 3. The software developed assumes that the processed signals are available to take the necessary decision. The following scheme is suggested for processing the signals available at the input of the indoor equipment.

5.1.2 Proposed Signal Processing Scheme for Axel Counting

Proposed signal processing of each output of the track transducer is given schematically in Fig. 5.1. This uses coherent demodulation of AM signal available at the indoor equipment. In this coherent demodulation PLL is used for tracking the carrier signal.

A major advantage of proposing PLL based coherent AM demodulation is that it track the 5 KHz signal even the oscillator drifts, due to various environmental conditions.

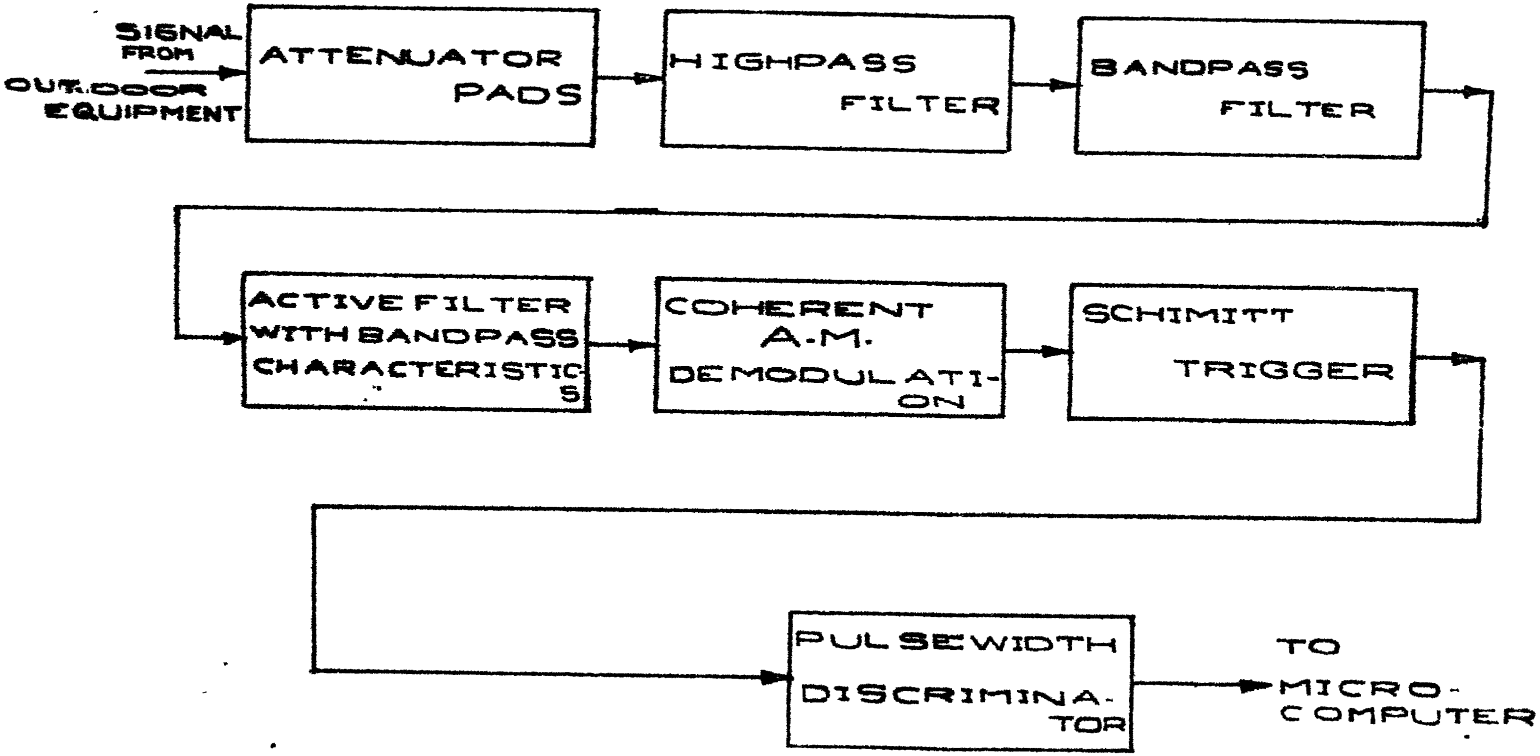


FIG.5.1. PROPOSED SIGNAL PROCESSING SCHEME

5.1.3 Basic Approach Involved in Axle Counting

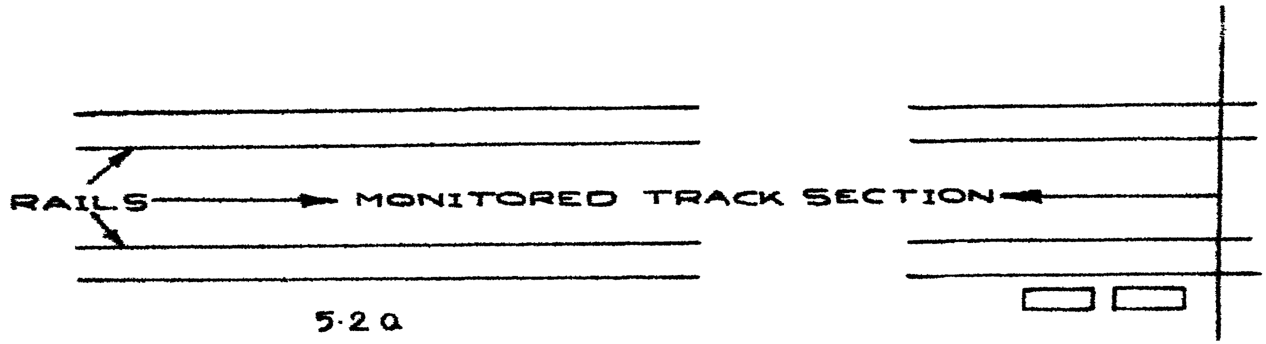
Fig. 5.2 shows a length of track monitored with one pair of transducers at one end. The relative positions of the transitions with respect to each other of the waveforms A and B, which are the outputs of the transducers A and B respectively contain the complete information regarding the movement of an axle across the transducer - pair and the direction.

Eight unique events are shown corresponding to a transition on one waveform and a level in the other waveform, in Tables of Fig. 5.2. These events are labelled In1, IN2, OUT1, OUT2.

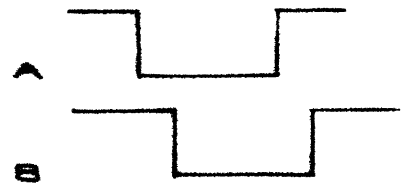
The system must identify two types of train movements on the track - through running and shunting. Four cases are enumerated below corresponding to shunting and through running. The sequence of events that would occur in the waveforms A and B are given in Fig. 5.2.

(Case 1) : Only one track transducer is affected by the wheel (Fig. 5.3a).

partial shunting (Case 2) : The signal of track transducer 'A' is dipped first and this is followed by 'B'. The wheel now draws back, clearing transducer 'B' first and finally transducer 'A' is also cleared. This corresponds to shunting movement into the track section and back without getting fully into

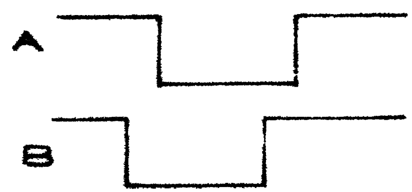


5·2 a



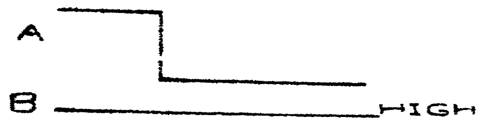
A	B	COUNT TO BE INCREMENTED
↓	H	IN1
L	↓	IN2
↑	L	IN1
H	↑	IN2

5·2 b INDICATION FOR TRAIN ENTERING



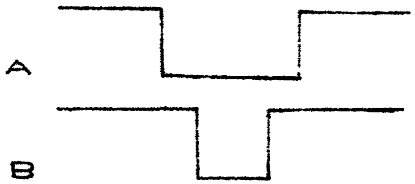
A	B	COUNT TO BE INCREMENTED
↓	L	OUT1
H	↓	OUT2
↑	H	OUT1
L	↑	OUT2

5·2 C INDICATION FOR TRAIN LEAVING



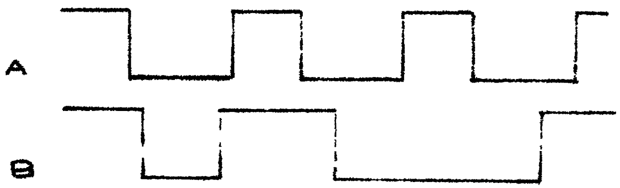
IN1	IN2	OUT1	OUT2	SIGNAL
1	–	–	–	ENGAGED

5·3a



IN1	IN2	OUT1	OUT2	SIGNAL
1	1	1	1	CLEAR

5·3b PARTIAL SHUNTING



IN1	IN2	OUT1	OUT2	SIGNAL
1+1+1	1+1	1+1+1	1+1	CLEAR

5·3c SHUNTING

FIG.5.3 VARIOUS TRAIN MOVEMENTS

Shunting (Case 3) : The above movement is continued further than case 2 to clear transducer 'A' but not 'B'. The wheel now moves back in opposite direction reoccupying 'A' and finally clears both 'A' and 'B'. This is the case of shunting (Fig. 5.3c).

Through running (Case 4) : Both A and B are occupied and cleared successively.

The status of the track, CLEAR or ENGAGED, is indicated based on the number of occurrences of the events IN1, IN2, OUT1, OUT2; when IN1 equals OUT1 and IN2 equals OUT2 CLEAR signal is given, otherwise ENGAGED signal is given.

5.2 HOTBOX DETECTION

A conventional infrared hotbox detector is proposed. The output of the detector is transmitted to the indoor equipment when this signal exceeds a pre-set threshold, an indication is given to the microcomputer. The microcomputer then having been interrupted announces the occurrence of a hotbox and indicates the number of the axle to which it corresponds.

Certain assumptions are made in the implementation of the software for the hotbox detection system. These are given below along with the proposed layout of the transducers.

5.2.1 Assumptions

Since both the hotbox detection system and the axle

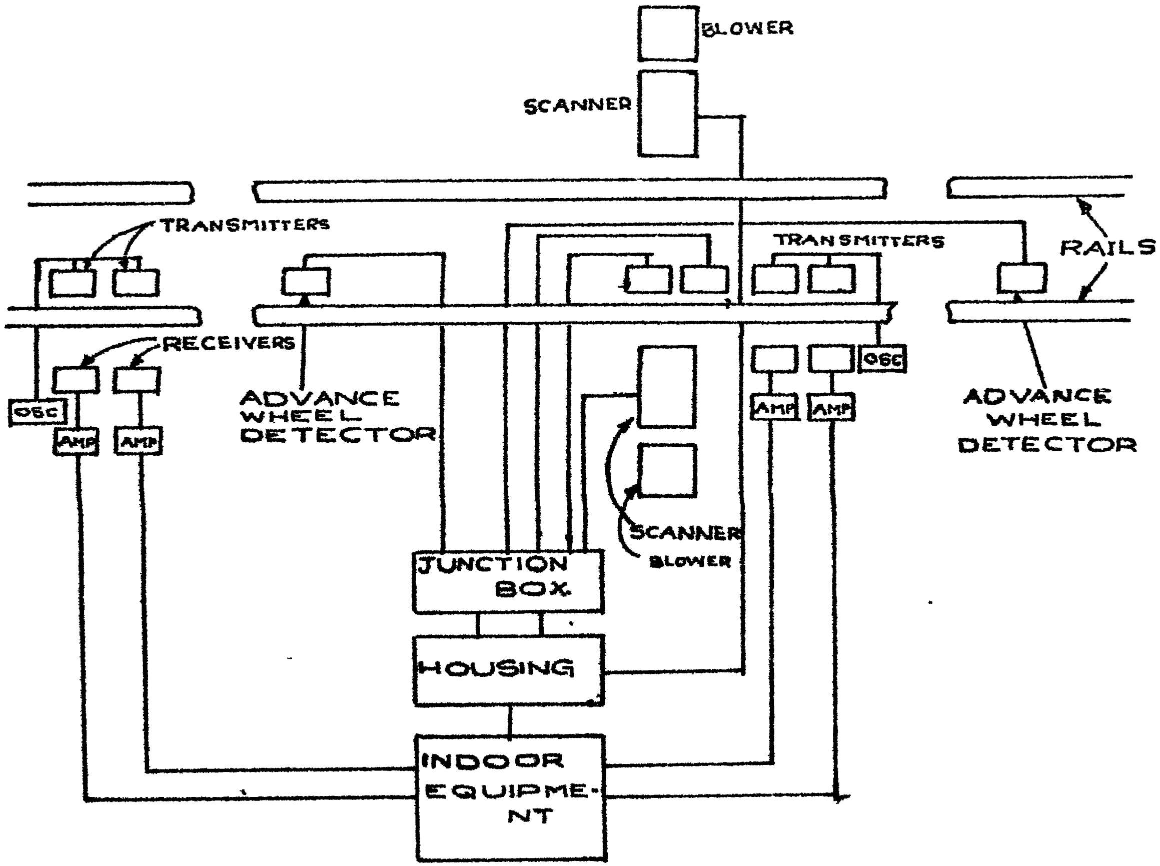


FIG 5.4 PROPOSED LAYOUT OF THE TRANSDUCERS

counting system are implemented through the same software, the following assumptions are made in the implementation of the hotbox detection system.

1. Hot axle transducers are kept at one end of [redacted] track that is maintained for axle counting system, s[redacted] it is sufficient to detect the hotbox at one end.
2. Hot axles are detected for through running only. [redacted]s expected that a hotbox does not occur for trains in shunting as they move very slowly.
3. It is assumed that hotbox detector is placed by the si[redacted] of the axle counting transducer pair.

5.2.2 Proposed Layout

A proposed layout of the axle counting transducers and the hotbox detector corresponding to a section of the track is shown schematically in Fig. 5.4.

CHAPTER 6

SOFTWARE DETAILS

Software is developed for a combined system of axle counting and hotbox detection. The software is developed for Motorola 6800 microprocessor based system. Although any other microprocessor can meet the requirements, M6800 is chosen because of the availability of its software development system. The developed software takes care of four detection point , axel counting system. The system provides a visual information of the movement of a train on the track at a remote location, say the control room.

From the schematic diagram of Fig. 6.1 it is seen that eight processed signals from four axle counting transducer pairs are given to the logic that generates a pulse whenever a change occurs in the status of the transducer outputs. This pulse is given to one of the interrupt pins of the Peripheral Interface Adapter (PIA), that is programmed for a high to low transition to produce an interrupt to the Microprocessor Unit (MPU). The output from hotbox ax detector and lock indicator output are given to another pair of interrupt pins of the PIA. Whenever, an interrupt is recognised MPU checks the source of the interrupt and processes it as described in the subsequent sections of this chapter.

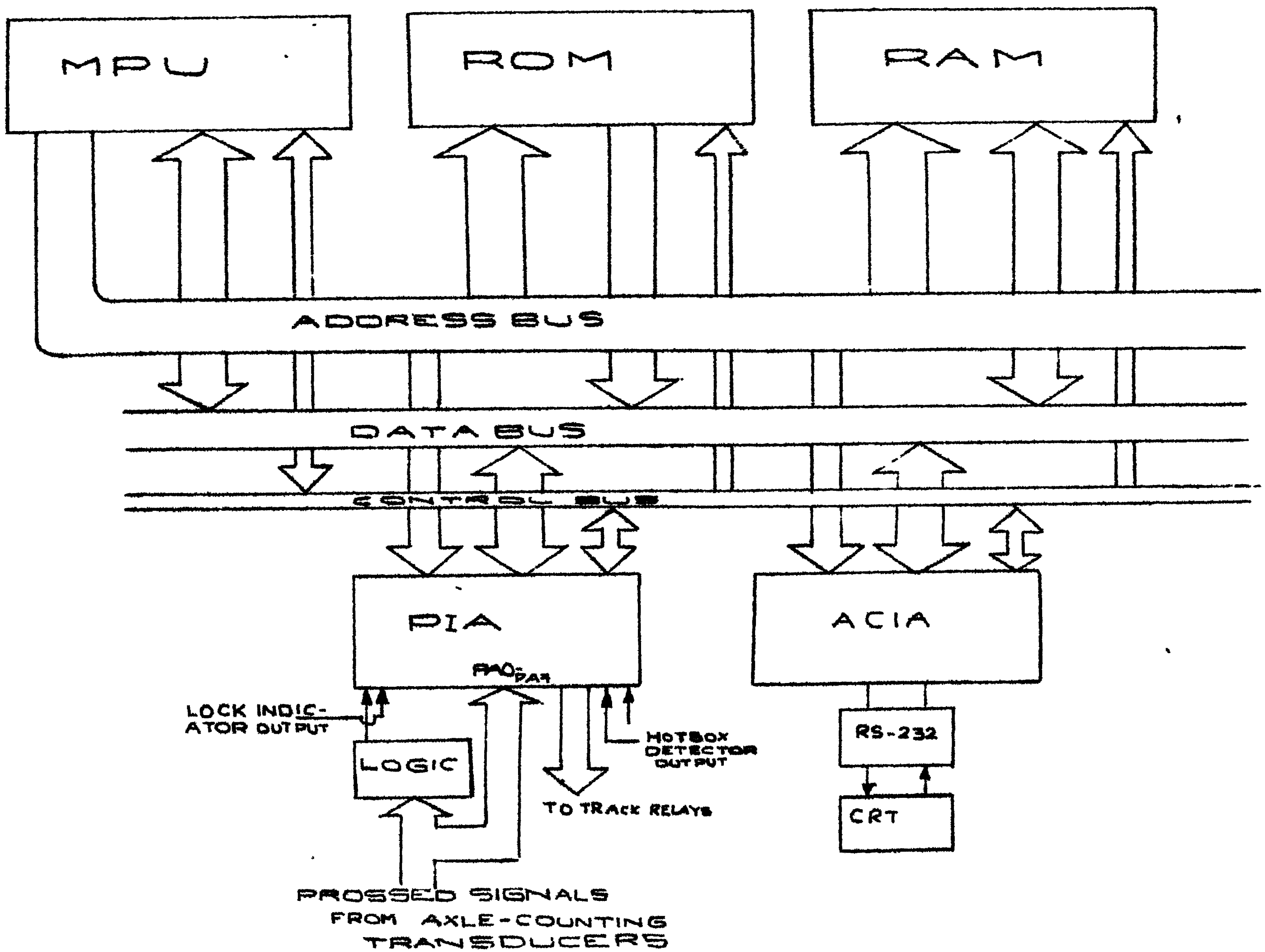


FIG.6.1 SCEMATIC DIAGRAM OF THE MICRO-COMPUTER

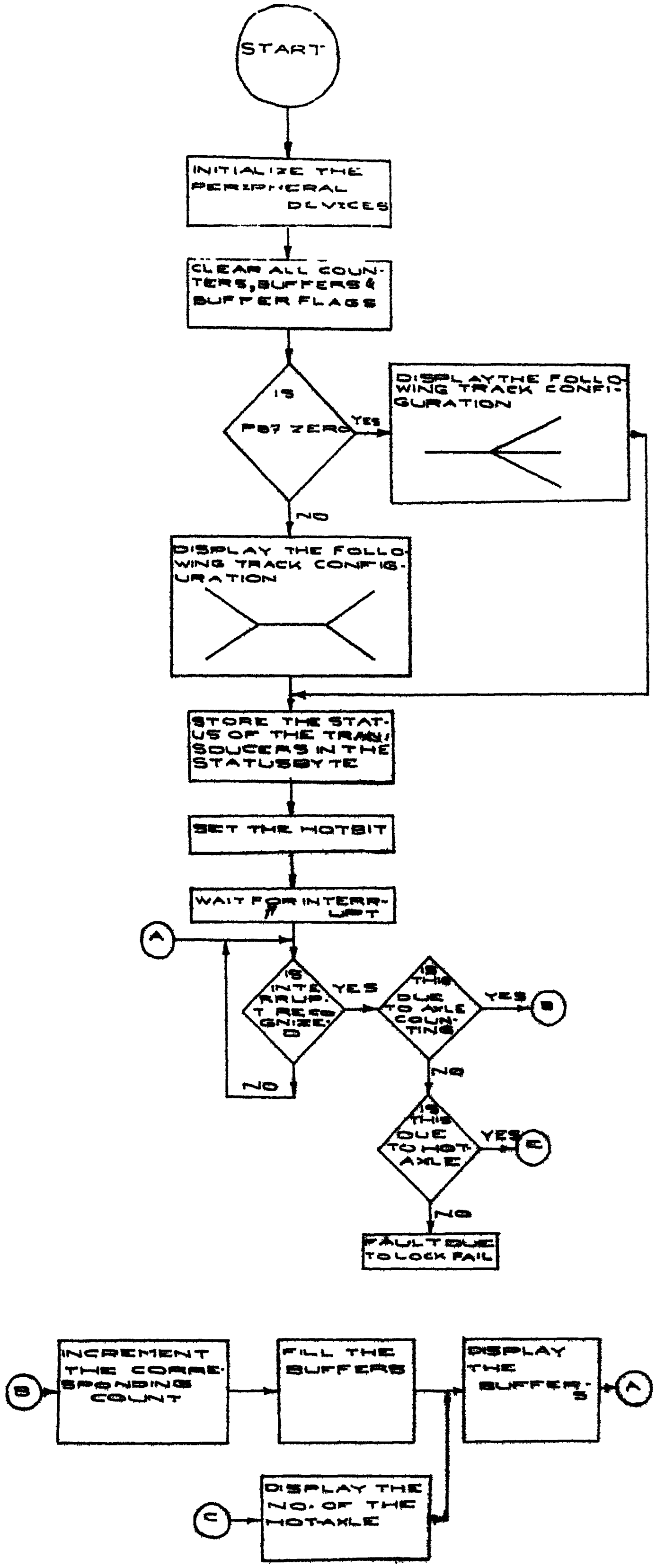


FIG.6.2 MAIN FLOW-CHART

A brief flow chart of the developed software is given in Fig. 6.2. At the outset, the system initializes the peripherals, and clears the buffers and the counters. Then the appropriate track configuration is displayed with a message 'TRACK IS CLEARED'. Afterwards the MPU waits for an interrupt. If an interrupt is recognised, it checks for the source of the interrupt, and goes to the appropriate routine depending upon the source of the interrupt and does the necessary action as described in the subsequent sections. Then, it goes to the display routine whenever there is no interrupt and starts displaying the contents of the buffer. During display, if an interrupt is recognized it attends to the interrupt routine, storing the present status and then comes back to the original display routine with the help of the stored status. The detailed discussion is given in the subsequent sections.

6.1 INITIALIZATION

In the initialization-routine, PIA is initialized depending on the requirements on the inputs available and outputs required.

The M6800 PIA provides a flexible method of connecting byte-oriented peripherals to the MPU. The PIA, while relatively complex itself, permits the MPU to handle a wide variety of equipment types with minimum additional logic and simple programming. An Input/Output Diagram of the MC6820 is shown in Fig. 6.3.

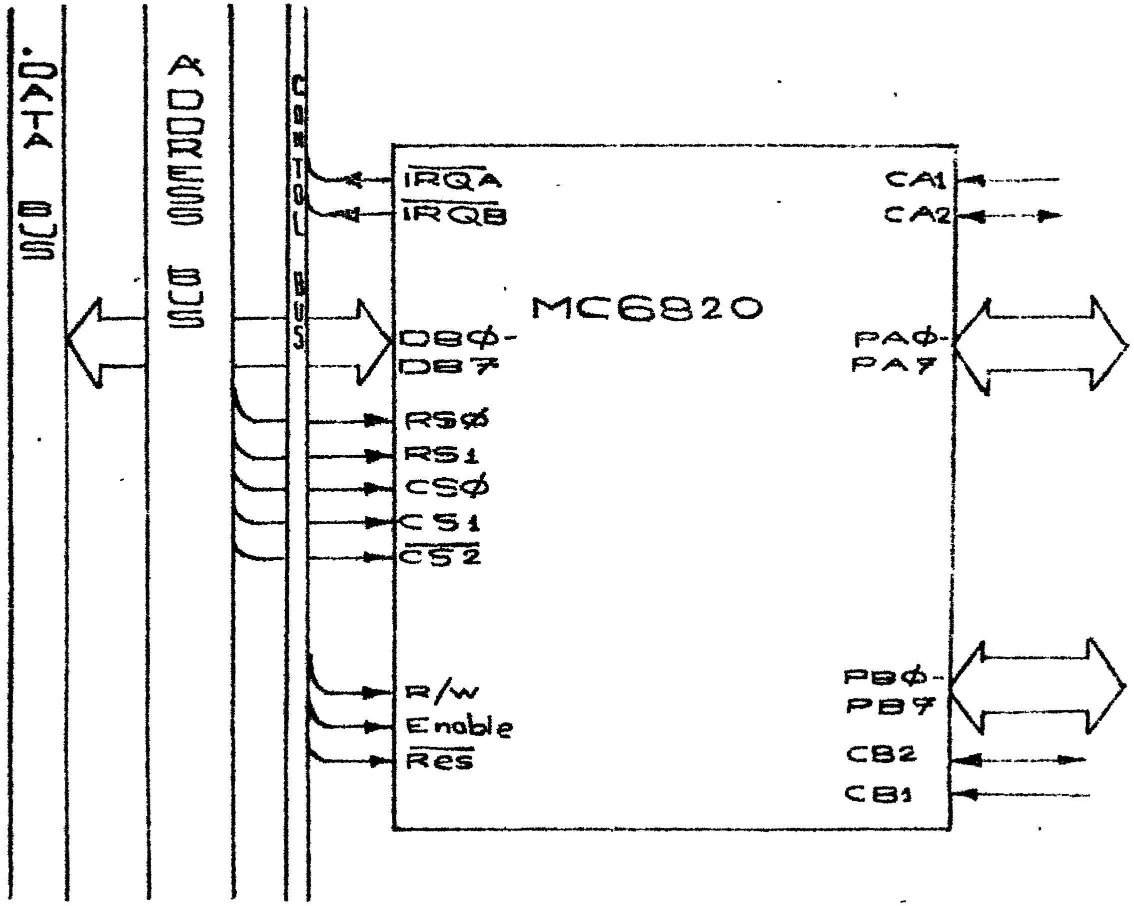


FIG.6.3 MC6820PIA I/O DIAGRAM

Data flows between the MPU and the PIA on the System Data Bus via eight bi-directional data lines DO through D7. The direction of data flow is controlled by the MPU via the Read/Write input to the PIA.

The 'MPU side' of the PIA also includes three chip select lines, CSO, CS1 and CS2, for selecting a particular PIA. Two addressing inputs RSO and RS1, are used in conjunction with a control bit with the PIA for selecting specific registers in the PIA. The MPU can read or write into the PIA's internal registers by addressing the PIA via the system Address Bus, using these five input lines and the R/W signal. From the MPU's point of view each PIA is simply four memory locations that are treated in the same manner as any other read/write memory.

The MPU also provides a timing signal to PIA via the Enable input. The Enable (E) pulse is used to condition the PIA's internal interrupt control circuitry and for the timing of the peripheral control signals. Since all data transfers take place during the φ_2 portion of the clock cycle, the Enable pulse is normally φ_2.

The 'Peripheral side' of the PIA includes two 8 bit-bidirectional data bus (PAO-PA7 and PBO-PB7) and four interrupt/control lines CA1,CA2,CB1 and CB2. All of these lines on the 'Peripheral side' of the PIA are compatible with Standard TTL logic.

An expanded Block Diagram of the PIA is shown in Fig. 6.4. Internally, the PIA is divided into two symmetrical independent register configurations. Each half has three main features : an output register, a control register and a Data Direction Register. It is these registers that the MPU treats as memory location i.e., they can be either read from or written into. The output and Data Direction Registers on each side represent a single memory location to the MPU. Selecting between them is internal to the PIA and is determined by a bit in their control register.

The Data Direction Registers (DDR) are used to establish each individual peripheral bus line as either an input or an output. This is accomplished by having MPU write 'ones' or 'zeros' into the eight bit position of the DDR. Zeros or ones cause the corresponding peripheral data lines to function as inputs or outputs, respectively.

The Output Registers, ORA and ORB, when addressed , store the data present on the MPU Data Bus during an MPU write operation. This data will also appear on those peripheral lines that have been programmed as outputs. If a peripheral lines has been programmed as an input, the corresponding bit position of the output register can still be written into by the MPU, however, the data will be influenced by the external signal applied on that peripheral data line.

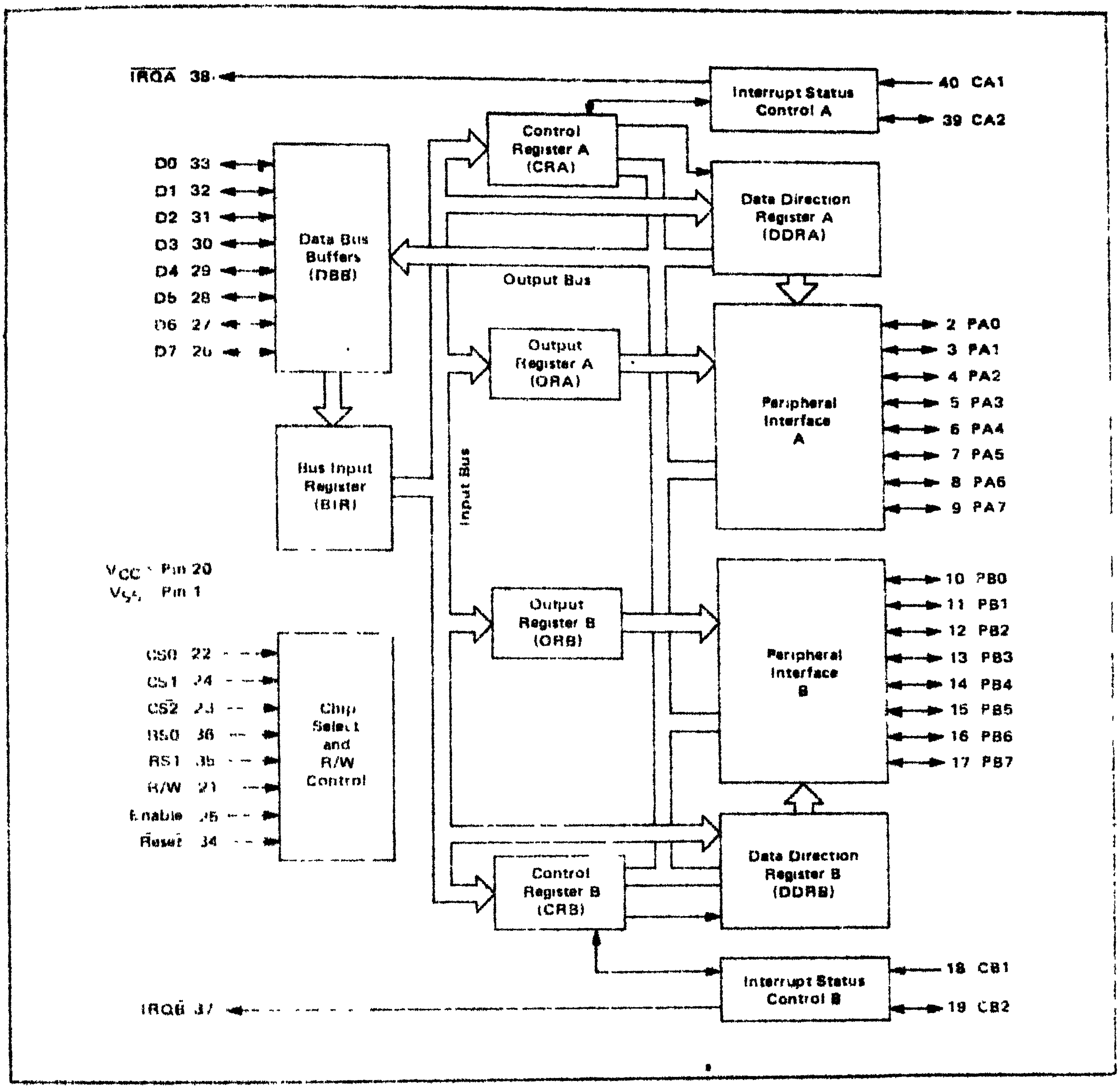


FIGURE 6·4 MC6820 PIA — Block Diagram

Determine Active CA1 (CB1) Transition for Setting Interrupt Flag IRQA(B)1 – (bit b7)

b1 = 0 : IRQA(B)1 set by high-to-low transition on CA1 (CB1).

b1 = 1 : IRQA(B)1 set by low-to-high transition on CA1 (CB1).

CA1 (CB1) Interrupt Request Enable/Disable

b0 = 0 Disables IRQA(B) MPU Interrupt by CA1 (CB1) active transition.[1]

b0 = 1 Enable IRQA(B) MPU Interrupt by CA1 (CB1) active transition.

1. IRQA(B) will occur on next (MPU generated) positive transition of b0 if CA1 (CB1) active transition occurred while interrupt was disabled.

IRQA(B) 1 Interrupt Flag (bit b7)

Goes high on active transition of CA1 (CB1). Automatically cleared by MPU Read of Output Register A(B). May also be cleared by hardware Reset.

b7	b6	b5	b4	b3	b2	b1	bϕ
IRQA(B)1 Flag	IRQA(B)2 Flag	CA2(CB2) Control			DDR Access	CA1(CB1) Control	

IRQA(B)2 Interrupt Flag (bit b6)

CA2 (CB2) Established as Input (b5 = 0) Goes high on active transition of CA2 (CB2). Automatically cleared by MPU Read of Output Register A(B). May also be cleared by hardware Reset.

CA2 (CB2) Established as Output (b5 = 1) IRQA(B)2 = 0, not affected by CA2 (CB2) transitions.

Determines Whether Data Direction Register Or Output Register is Addressed

b2 = 0 : Data Direction Register selected.

b2 = 1 Output Register selected.

CA2 (CB2) Established as Output by b5 = 1

b5	b4	b3
1	0	

(Note that operation of CA2 and CB2 output functions are not identical)

→ CA2

b3 0 Read Strobe With CA1 Restore

CA2 goes low on first high-to-low E transition following an MPU Read of Output Register A, returned high by next active CA1 transition.

b3 1 Read Strobe with E Restore

CA2 goes low on first high-to-low E transition following an MPU Read of Output Register A, returned high by next high-to-low E transition.

→ CB2

b3 = 0 Write Strobe With CB1 Restore

CB2 goes on low on first low-to high E transition following an MPU Write into Output Register B, returned high by the next active CB1 transition.

b3 = 1 : Write Strobe With E Restore

CB2 goes low on first low to-high E transition following an MPU Write into Output Register B, returned high by the next low to high E transition.

b5	b4	b3
1	1	

→ Set/Reset CA2 (CB2)

CA2 (CB2) goes low as MPU writes b3 = 0 into Control Register.

CA2 (CB2) goes high as MPU writes b3 = 1 into Control Register.

CA2 (CB2) Established as Input by b5 = 0

b5	b4	b3
0		

→ CA2 (CB2) Interrupt Request Enable/Disable

b3 = 0 Disables IRQA(B) MPU Interrupt by CA2 (CB2) active transition.[1]

b3 = 1 . Enables IRQA(B) MPU Interrupt by CA2 (CB2) active transition.

1 IRQA(B) will occur on next (MPU generated) positive transition of b3 if CA2 (CB2) active transition occurred while interrupt was disabled

→ Determines Active CA2 (CB2) Transition for Setting Interrupt Flag IRQA(B)2 – (bit b6)

b4 = 0 : IRQA(B)2 set by high-to-low transition on CA2 (CB2).

b4 = 1 . IRQA(B)2 set by low-to-high transition on CA2 (CB2).

FIGURE 6·5 PIA Control Register Format

During an MPU Read operation, the data present on peripheral lines programmed as inputs is transferred directly to the system Data Bus. Due to differing circuitry, the results of reading positions programmed as outputs differ slightly between sides A and B of the PIA. On the B side, there is three-state buffering between Output Register B and peripheral lines such that the MPU will read the current contents of ORB for those bit positions programmed as outputs. During an MPU Read of the A side, the data present on the peripheral lines will affect the MPU Data Bus regardless of whether the lines are programmed as outputs or inputs. The bit positions in ORA designated as outputs will be read correctly only if the external loading on the peripheral lines is within the specifications for one TTL load. That is, logic one used could be read as a logic zero if excessive loading reduced the voltage below 2.0 Volts.

The two control registers, CRA and CRB, allow the MPU to establish and control the operating modes of the peripheral control lines CA1, CA2, CB1 and CB2. It is by means of these four lines that control information is passed back and forth between the MPU and peripheral devices. The control word format and a summary of its features is shown in Fig. 6.5.

The following are the input signals available for processing :

1. Eight processed signals from the axle counter transducers.

2. One signal from the lock indicator output to be given to one of the interrupts pins of the PIA.
3. One signal from the hotbox detector output to be given to another interrupt pin of the PIA.
4. Another input which is produced by the logic, from the eight axle counter transducer signals for producing interrupts
5. A signal by whose status the processor would be able to decide upon the information about the track configuration at which transducers are installed.

The outputs to be provided from the PIA are :

1. to energize CLEAR relay to give CLEAR indication at the track side
2. to energize ENGAGED relay to give ENGAGED indication at the track side
3. to energize FAULT relay to give FAULT indication.

Therefore, it is necessary that three of the four interrupt pins of the PIA have to be enabled to produce an interrupt to the MPU. Although interrupt pins can be programmed to be active for any transition (high to low or low to high), they are programmed for high to low transition to be active. That is whenever a high to low transition is recognised on these pins an interrupt is generated by the PIA to the MPU. Eight pins of the peripheral side A of the PIA are programmed as inputs and are given processed signals

of the axle counter transducers. Pin PB7 of the peripheral side B is programmed as input whose status gives an information about the track configuration to the processor. All other pins of the peripheral side B of the PIA are programmed as outputs out of which PBO gives ENGAGED indication, PB1 gives CLEAR indication and PB2 gives FAULT indication. That is whenever CLEAR indication is to be given PB1 is made logical are by the MPU. Similarly, PBO for the ENGAGED signal PB2 for the FAULT signal are made 'logical 1'. The algorithm for initialization is given below.

Initialization algorithm :

1. Select the control registers of A side and B side (select PIACRA, PIACRB)
2. Select the Data Direction registers of sides A and B side (PIADRA, PIADRB) by writing be bit of PIACRA, PIACRB as zero (Fig. 6.5)
3. Make the PAO through PA7 pins as inputs by writing all bits of PIADRA as 'zeros'.
4. Make PBO through PB6 as outputs and PB7 as input by writing all bits of PIADRB as 'ones' except eighth bit.
5. Select PIACRA and PIACRB.
6. Select both the output registers and make the interrupt pins to be active for high to low transition by writing the bits of PIACRA, PIACRB accordingly.

The actual program can be seen from the initialization routine in the program listing given at the end of the thesis.

6.2 CLEARING THE COUNTS AND BUFFERS

After the initialization is over the program has to clear the screen, and the buffers and counters maintained. In random access memory (RAM) these counters and buffers are maintained. These counters and buffers are maintained in consecutive locations in the RAM so that a small loop of about 5 lines of program can clear them. In the RAM two types of counters are maintained. One is four sets of local counters and the other is global counters. Each set of the local counters contains local IN1. local IN2, local OUT1, local OUT2 in it and these are incremented only when the MPU decides that the count generated is due to its corresponding transducer pair. Global counters also contains global IN1, global IN2, global OUT1 and global OUT2 in it and are incremented correspondingly whenever any of the corresponding local count is incremented. That is whenever any of the local IN1 is incremented global IN1 is incremented, whenever any of the local IN2 is incremented global IN2 is incremented and so on. In the program five buffers are maintained for storing the information of the counts to be displayed by the display routine. The buffers contain the following information.

1. The code for the graphics cursor position where the counts are to be displayed on the CRT screen.
2. IN and OUT counts to be displayed in binary form.
3. Code for the message to be sent to the terminal about the occupancy of the track section.

6.3 DISPLAYING THE TRACK CONFIGURATION

After clearing the screen, the buffers and the counters, the program checks the status of the pin PB7 of the PIA. If it is zero the pictorial representation of track configuration shown in Fig. 6.6a is displayed with the message 'TRACK IS CLEARED',otherwise the track configuration shown in Fig. 6.6b is displayed on the CRT terminal. After displaying the appropriate track configuration the processor stores the status of the track transducers outputs in a status byte maintained in the RAM and then waits for an interrupt.

When an interrupt is recognised processor checks the source of the interrupt by checking the 8th and the 7th bits of PIACRA and PIACRB. If the eighth bit of PIACRA is set then processor branches over to the axle counting routine. If the 7th bit of PIACRA is set it knows that the interrupt is due to lock indication failure and gives a fault indication. If the 8th bit of PIACRB is set then it jumps to the hotaxle routine.

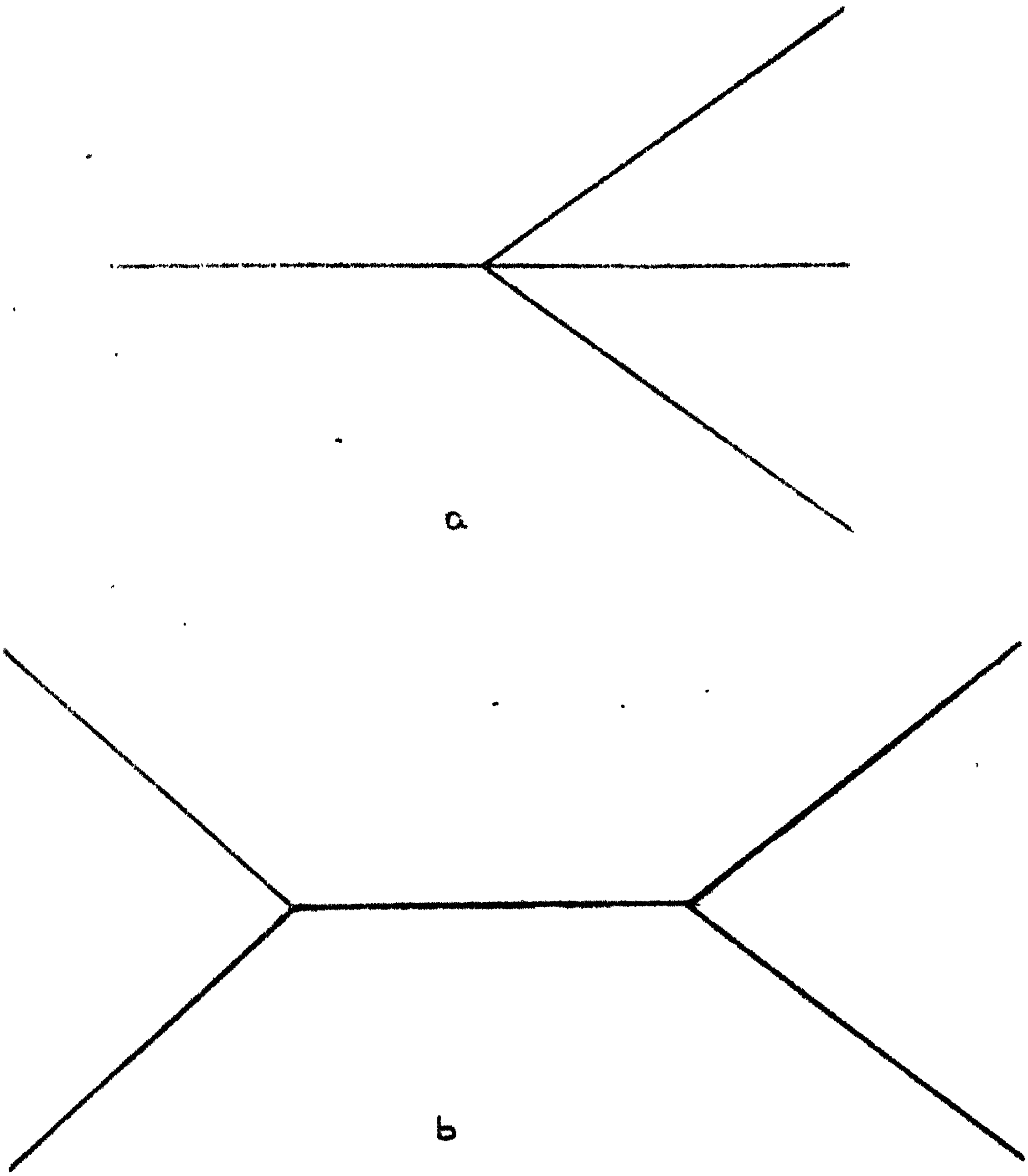


FIG6.6 PICTORIAL REPRESENTATION OF THE TWO POSSIBLE TRACK-SECTIONS

6.4 AXLE COUNTING ROUTINE

After recognising that the interrupt is generated due to the axle counting transducers, processor takes the present status of the track transducers and does 'exclusive-OR' with the previous status stored in the status byte to find the particular transducer that has changed its status due to the wheel of the train. At the same time it makes PBO 'logical1' to indicate that the track is ENGAGED. Then the particular bit of the status byte corresponding to the changed status is updated accordingly. Afterwards the processor checks for the status of the other transducer in the transducer pair and increments the corresponding Global count. Then it checks for the vacant buffer and fills the first byte of the buffer with the code corresponding to the graphic cursor position of the local count to be displayed. In the RAM one buffer flag corresponding to each buffer is maintained to indicate whether that buffer is full or vacant. A buffer flag is zero indicates the vacancy and new data can be entered, otherwise the buffer is full. Then it increments the corresponding local count and fills the consecutive bytes of the buffer with the binary value of the local count to be displayed. Finally, last byte of the buffer is filled with the code corresponding to the message to be displayed on the CRT terminal. Then the buffer flag is cleared. If this byte is zero the message 'TRACK IS ENGAGED' is displayed, otherwise 'TRACK IS CLEARED' is

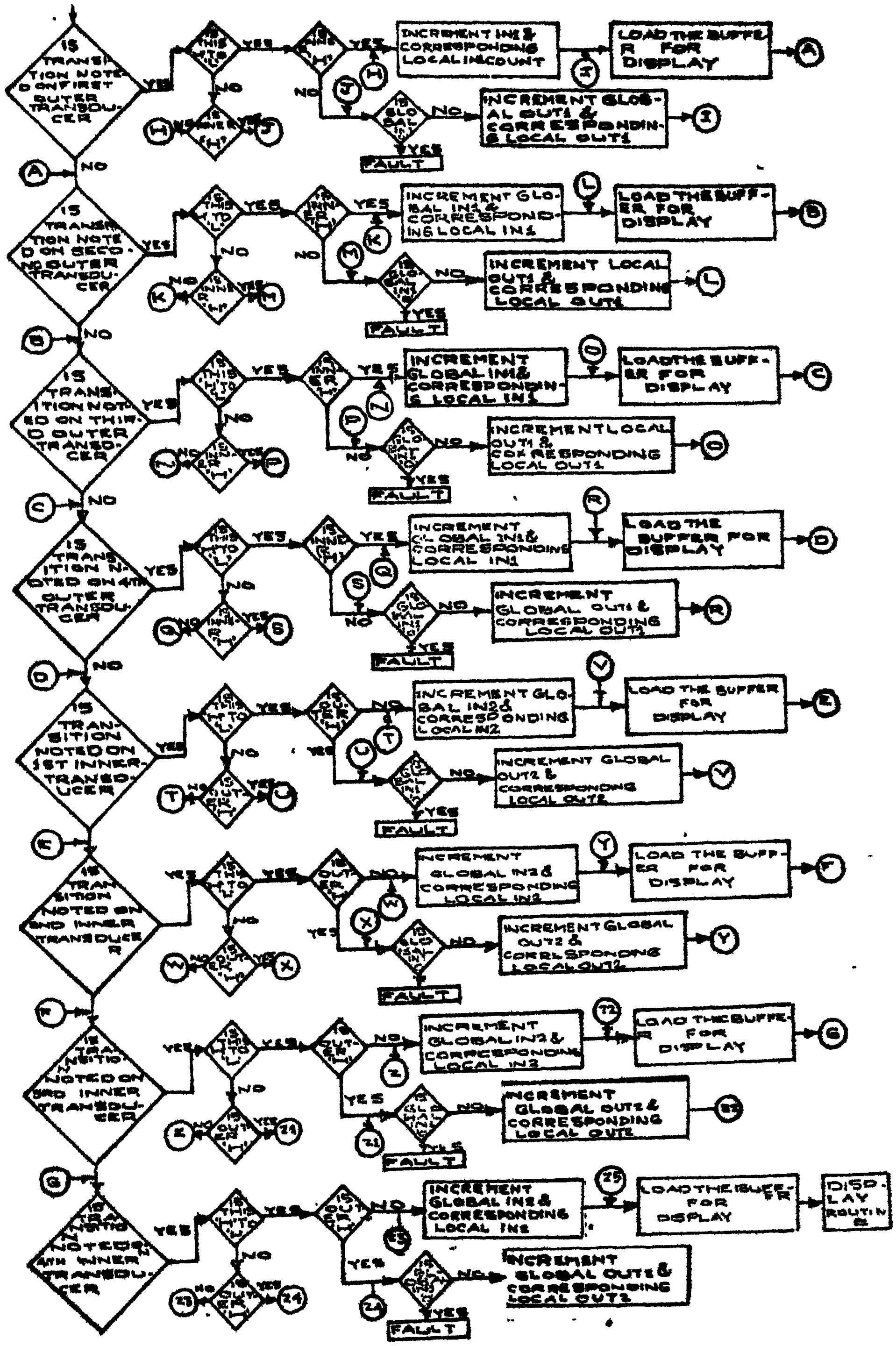


FIG 6.1 DETAILED FLOWCHART OF AXLE-COUNTING

displayed. If the track is cleared PB7 is made 'logical1' indicating that the track is clear which energises 'CLEAR RELAY'. Before incrementing outcount the processor checks that the corresponding incount is zero or not. If it is zero it gives fault signal because without an incount, outcount cannot be registered. This shows some extraneous signal or some malfunctioning of the processor or peripherals.

After incrementing the appropriate count and filling the corresponding buffers the processor goes to the display routine and it starts displaying the counts and the message about the track status. After it completes displaying one buffer it clears the buffer flag indicating that new data can be loaded into it. In this processes of display if any interrupt is recognised the processor stops the display at that point storing the information about its status and attends to its interrupt routine and comes back to its original status and starts doing it. If again an interrupt is recognised similar action takes place. If all buffers are displayed and still interrupt is not recognised then processor waits for an interrupt. In displaying the count it changes the binary count stored to decimal count and displays. Shunting movement of a train can be interpreted if both IN count and OUT count are displayed at the same transducer. This count does not correspond to the exact number of wheels entered or left the track because one wheel can produce all

the count, whereas in through running this corresponds to the exact number of wheels that have entered and left.

6.5 HOTBOX DETECTION ROUTINE

After recognising that the interrupt is due to[redacted] output from the hotbox detector, processor comes to this ro[redacted]e.

When first incount is registered in axle counting routine, processor checks whether this incount is genera[redacted] by the axle counting transducer kept by the side of the hotbox detector. If not, 'Hotbit', which is maintained i[redacted] the RAM iscleared. This hotaxle detection routine first checks whether 'hotbit' is zero or not. If it is zero it assumes that hotzxle is produced when train is entering the track and it takes incount for displaying the number of wheel. Otherwise outcount is taken for displaying the exact number of wheel which is hot. Details can be seen from the programme listings given at the end of the thesis.

CHAPTER 7

CONCLUSIONS

The software is developed for a combined system of axle-counting and hotbox detection, assuming that the processed signals are available from the respective transducers.

The software has the following features :

1. It takes care of four detection point axle-counting system and can easily be modified for more detection points.
2. It has the maximum counting capacity of 2^{15} wheels, which can be extended further.
3. It provides a visual information of the status of the track-section of interest.
4. In the fail safety point of view, although it can not pinpoint the particular component in the system that is mal-functioning, it provides a 'FAULT' indication along with the 'ENGAGED' signal whenever there is a lock-failure or some other failure producing logically in-compatible count.

The system has been tried out successfully by simulating real time signals using a toy train system. However, a more thorough testing of the performance of the system in an actual environment is required.

The following features can be incorporated for the further improvement of the present system.

1. To facilitate a convenient visual display for the status of the track, it is suggested that the track section that is engaged is displayed differently, for example by a dotted line, compared to the section that is clear. At the approaching point for the engaged track section only the incount need be displayed and at the outgoing point the outcount.

2. After the completion of the display function, the processor can be used for self-check of the system, before an interrupt is recognised. This ensures improved fail-safety and better utilization of the microprocessor capabilities.

3. Instead of making the decision about the occurrence of the hotbox on a pre-set threshold, it is preferable to record the output of the hotbox detector corresponding to the each of the bearings and suitably process them. A decision based on such a scheme will result in lesser false alarms, [9] because in this case the threshold will be set according to the actual average conditions of the bearings of the particular train, rather than a global minimum threshold set apriori.

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APPENDIX

The simulated signals are generated using photodetectors and light sources. When train passes over the light source the required transition is produced.

The circuit diagram used for interrupt generation is given in Fig. A-1. Only two detection point axle counting system is simulated because of the nonavailability of cross-overs. The signals from the transducers are given to one port of 4-bit magnitude comparator (7485). The same signals are given to D-flip flops, whose outputs are given to the other port of the comparator. 'A=B' output is given to a monoshot and clock pin of D-flip flops through AND gate whose other input is output of a oscillator. The details can easily be understood from the circuit diagram.

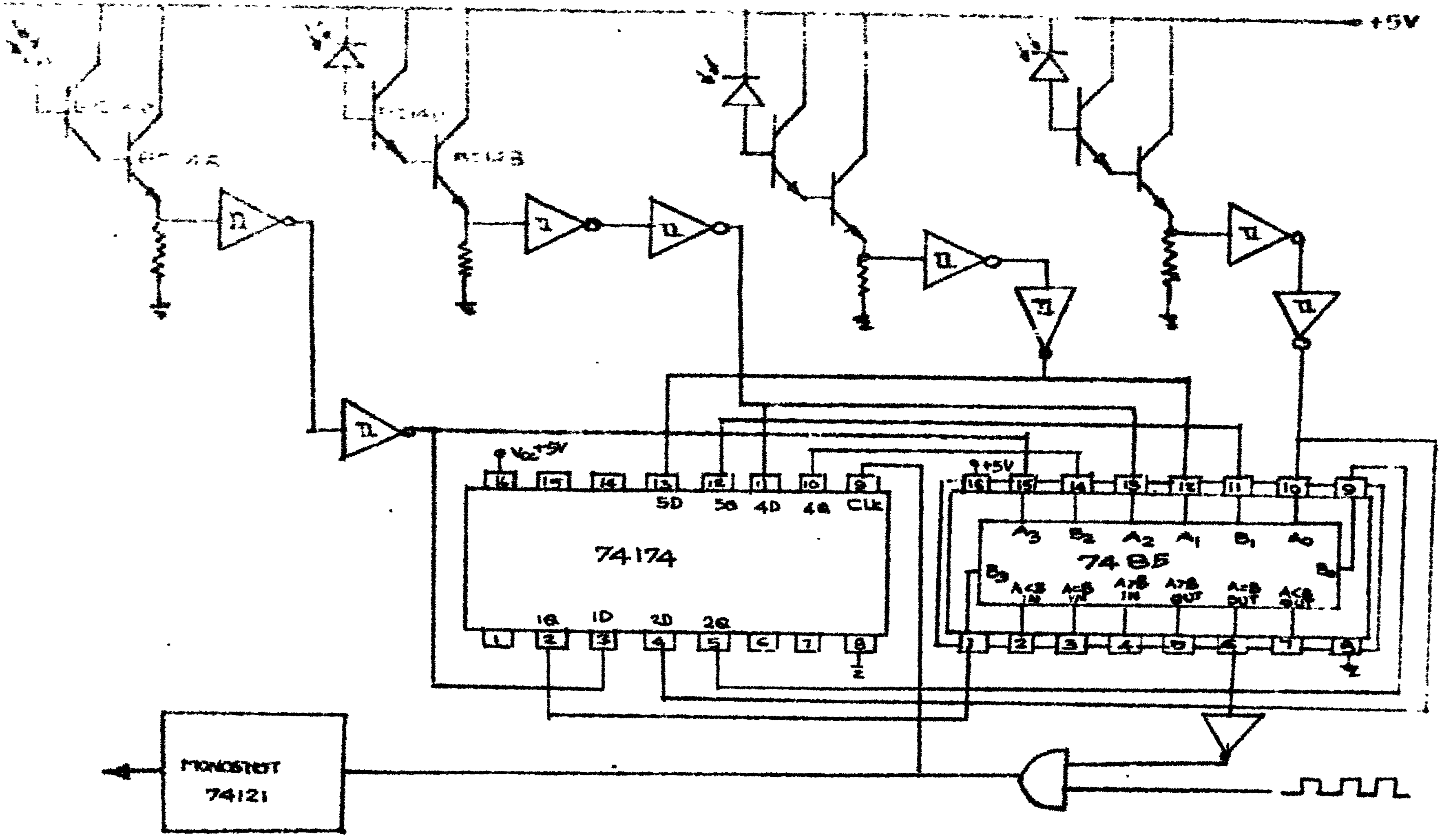

FIG A1. INTERRUPT GENERATION CIRCUIT

****

A S S E M B L Y - L I S T I N G

****

```
FBCE            ACIACR   EQU     $FBCE
FBCE            ACIASR   EQU     $FBCE
FBCF            ACIADR   EQU     $FBCF
0030            STOREA   EQU     $0030
FBC9            PIACRA   EQU     $FBC9
FBC8            PIAORA   EQU     $FBC8
FBC8            PIADRA   EQU     $FBC8
FBCA            PIAORB   EQU     $FBCA
FBCA            PIADRB   EQU     $FBCA
FBCB            PIACRB   EQU     $FBCB
0000            STBYT    EQU     $0000
0001            CNT1     EQU     $0001
0002            CNT2     EQU     $0002
0003            IN11     EQU     $0003
0004            IN1      EQU     $0004
0005            IN22     EQU     $0005
0006            IN2      EQU     $0006
0007            OUT11    EQU     $0007
0008            OUT1     EQU     $0008
0009            OUT22    EQU     $0009
000A            OUT2     EQU     $000A
002B            CHBYT1   EQU     $002B
002C            CHBYT2   EQU     $002C
002D            CHBYT3   EQU     $002D
002E            CHBYT4   EQU     $002E
002F            HTBIT    EQU     $002F
0003            CLRIND   EQU     $0003
002A            CLREII   EQU     $002A
E009            INDEX    EQU     $E009
E000            INDEX1   EQU     $E000
0031            INDEX2   EQU     $0031
0033            SAVEA    EQU     $0033
0034            SAVEX1   EQU     $0034
0036            BFLIND   EQU     $0036
0040            BUF1PT   EQU     $0040
0041            BUF2PT   EQU     $0041
0042            BUF3PT   EQU     $0042
0043            BUF4PT   EQU     $0043
0044            BUF5PT   EQU     $0044
0045            BUFIND   EQU     $0045
0064            BUFEND   EQU     $0064
0047            1STBUF   EQU     $0047
004D            SNDBUF   EQU     $004D
0053            THDBUF   EQU     $0053
0059            FRTBUF   EQU     $0059
005F            FFHBUF   EQU     $005F
FFF8            INTVCT   EQU     $FFF8
E000                     ORG     $E000
E000                     RMB     1
E001  80 40 20           FCB     $80,$40,$20,$10,$08,$04,$02,$01
 E009                     RMB     2
E00B  00 0B 00           FCB     $00,$0B,$00,$13,$00,$1B,$00,$23
 E013  0D 0A FF  NEG1     FCB     $0D,$0A,$FF
```

```
E041  01 03       HTIT     FCB     $01,$03
                  **       FIGRE1 -- GRAPHICS DATA FOR FIGURE ONE
E043  1B 2A       FIGRE1   FCB     $1B,$2A
E045  70 61 32             FCC     'PA250,150 550,150A450,150 550,250A
0,50Z'
E076  1B 2A                FCB     $1B,$2A
E078  64 6B 32             FCC     'DK200,2000S'
E083  1B 2A                FCB     $1B,$2A
E085  6D 34 61             FCC     'M4A2MIN36PIN  OUT'
E096  1B 2A                FCB     $1B,$2A
E098  64 6B 35             FCC     'DK500,3000SIN  OUT'
E0AA  1B 2A                FCB     $1B,$2A
E0AC  64 6B 35             FCC     'DK500,2000SIN  OUT'
E0BF  1B 2A                FCB     $1B,$2A
E0C1  64 6B 35             FCC     'DK500,500SIN  OUT'
E0D1  1B 2A                FCB     $1B,$2A
E0D3  6D 34 61             FCC     'M4A1MIN36F'
E0DD  1B 2A                FCB     $1B,$2A
E0DF  64 54                FCC     'DT'
E0E1  FF                   FCB     $FF
                  **       FIGRE2 -- GRAPHICS DATA FOR FIGURE TWO
E0E2  1B 2A       FIGRE2   FCB     $1B,$2A
E0E4  70 61 31             FCC     'PA150,250 250,150 450,150 550,250A
E10D  32 35 30             FCC     '250,150A450,150 550,50Z'
E124  1B 2A                FCB     $1B,$2A
E126  64 6B 31             FCC     'DK100,2000S'
E131  1B 2A                FCB     $1B,$2A
E133  6D 34 61             FCC     'M4A2MIN36PIN  OUT'
E144  1B 2A                FCB     $1B,$2A
E146  64 6B 35             FCC     'DK500,3000SIN  OUT'
E158  1B 2A                FCB     $1B,$2A
E15A  64 6B 31             FCC     'DK100,500SIN  OUT'
E16B  1B 2A                FCB     $1B,$2A
E16D  64 6B 35             FCC     'DK500,500SIN  OUT'
E17E  1B 2A                FCB     $1B,$2A
E180  6D 34 61             FCC     'M4A1MIN36F'
E18A  1B 2A                FCB     $1B,$2A
E18C  64 54                FCC     'DT'
E18E  FF                   FCB     $FF
                  **       CURS11 -- FIRST POSITION OF THE CURSOR
                   *                 OF THE FIRST FIGURE.
E18F  1B 2A       CURS11   FCB     $1B,$2A
E191  64 6B 32             FCC     'DK200,1800S'
E19C  FF                   FCB     $FF
                  **       CURS12 -- SECOND POSITION OF THE CURSOR
                   *                 OF THE FIRST FIGURE.
E19D  1B 2A       CURS12   FCB     $1B,$2A
E19F  64 6B 35             FCC     'DK500,1800S'
E1AA  FF                   FCB     $FF
                  **       CURS13 -- THIRD POSITION OF THE CURSOR.
E1AB  1B 2A       CURS13   FCB     $1B,$2A
E1AD  64 6B 35             FCC     'DK500,2800S'
E1B8  FF                   FCB     $FF
                  **       CURS14 -- FOURTH POSITION OF THE CURSOR.
E1B9  1B 2A       CURS14   FCB     $1B,$2A
E1BB  64 6B 35             FCC     'DK500,300S'
E1C5  FF                   FCB     $FF
```

```
                  **      CURS21 -- FIRST POSITION OF THE CURSOR
                   *                 OF THE SECOND FIGURE.
 F1C6  1B 2A      CURS21  FCB     $1B,$2A
F1C8  64 6B 31            FCC     'DK100,2800S'
F1D3  FF                  FCB     $FF
                  **      CURS22 -- SECOND POSITION OF THE CURSOR
                   *                 OF THE SECOND FIGURE.
 F1D4  1B 2A      CURS22  FCB     $1B,$2A
F1D6  64 6B 31            FCC     'DK100,300S'
F1E0  FF                  FCB     $FF
F1E1  20 20 20  BLANK     FCC     '    '
F1E5  FF                  FCB     $FF
                  **      CLROR1 -- DATA STORED FOR CLEARING THE
                   *                 COUNT DISPLAYED ON FIGURE ONE.
  F1E6  1B 2A      CLROR1  FCB     $1B,$2A
F1E8  64 6B 32            FCC     'DK200,1800S               '
  F202  1B 2A               FCB     $1B,$2A
F204  64 6B 35            FCC     'DK500,2800S               '
 F21E  1B 2A               FCB     $1B,$2A
F220  64 6B 35            FCC     'DK500,300S                '
 F23A  1B 2A               FCB     $1B,$2A
F23C  64 6B 35            FCC     'DK500,1800S               '
  F256  1B 2A               FCB     $1B,$2A
F258  64 54               FCC     'DT'
F25A  FF                  FCB     $FF
                  **      CLROR2 -- DATA STORED FOR CLEARING THE
                   *                 COUNT DISPLAYED ON FIGURE-TWO.
  F25B  1B 2A      CLROR2  FCB     $1B,$2A
F25D  64 6B 31            FCC     'DK100,2800S               '
  F277  1B 2A               FCB     $1B,$2A
F279  64 6B 35            FCC     'DK500,2800S               '
 F293  1B 2A               FCB     $1B,$2A
F295  64 6B 35            FCC     'DK500,300S                '
  F2AF  1B 2A               FCB     $1B,$2A
F2B1  64 6B 31            FCC     'DK100,300S                '
  F2CB  1B 2A               FCB     $1B,$2A
F2CD  64 54               FCC     'DT'
F2CF  FF                  FCB     $FF
                  **      CLRBYT -- 'CLEAR BYTE'
                   *                -- USED FOR CHECKING THE EMPTINESS
                   *                 -- OF THE TRACK SECTION.
 F2D0  FF          CLRBYT  FCB     $FF
                  **      CLEARD -- 'CLEARED'
                  *                 -- USED FOR SENDING THE MESSAGE
                   *                 -- 'TRACK IS CLEARED'.
  F2D1  1B 2A      CLEARD  FCB     $1B,$2A
F2D3  6D 34 61            FCC     'M4A2MIN3CR'
F2DD  1B 2A               FCB     $1B,$2A
F2DF  64 6B 31            FCC     'DK10,3500STRACK IS CLEARED'
  F2F9  1B 2A               FCB     $1B,$2A
F2FB  6D 34 61            FCC     'M4A1MIN3CR'
F305  1B 2A               FCB     $1B,$2A
F307  64 54               FCC     'DT'
F309  FF                  FCB     $FF
```

```
                              *                  -- 'TFACK IS ENGAGED'.
 E30A   1P 2A       ENGAGI  FCP       $1P,$2A
E30C  6D 24 61              FCC       'MAA2M1N3CF'
E316   1P 2A                FCP       $1P,$2A
E318  64 6P 21              FCC       'DK10,3F00STFACP IS ENGAGED'
 E332  1P 2A                FCP       $1P,$2A
E334  6D 24 61              FCC       'MAA1M1N3CF'
E33F   1P 2A                FCP       $1P,$2A
E340  64 54                 FCC       'DT'
E342  FF                    FCP       $FF
                         ** SCFCLF -- 'SCFEEN CLEAF'
                          *             -- USED FOR CLEAPING THE
                          *             -- GPAPHICS DISPLAY ON THE CFT.
  E343  1P 2A       SCPCLF  FCP       $1P,$2A
E345  64 41                 FCC       'DA'
E347  FF                    FCP       $FF
                         ** PUFFLT -- 'PUFFEF FAULT'
                          *             -- USED TO INDICATE BUFFEF
                           *             -- OVEPFLOW.
E348  42 55 46  PUFFLT  FCC       'PUFFEP OVEFFLOW'
 E357  FF                   FCP       $FF
                         ** INITPT -- INTIALIZATION FOUTINE
 E358  86 00       INITPT  LDA A    #$00
E35A  P7 FP C9              STA A    PIACPA
E35D  P7 FP CP              STA A    PIACPP
E360  C6 7F                 LDA P    #$7F
E362  P7 FP C8              STA A    PIADPA
E365  F7 FP CA              STA P    PIADPP
E368  86 0D                 LDA A    #$0D
E36A  P7 FP C9              STA A    PIACPA
E36D  P7 FP CP              STA A    PIACPP
E370  CE E3 43              LDX      #SCFCLF      CLEAPS THE SCFEEN
  E373  PD E7 CD             JSP      OUTSTF
E376  P6 FP CA              LDA A    PIAOPP
E379  85 80                 PIT A    #$80
E37P  27 08                 PEQ      FIG1
E37D  CE E0 E2              LDX      #FIGFE2
E380  PD E7 CD              JSP      OUTSTF
E383  20 06                 PPA      STAPT1
E385  CE E0 43  FIG1    LDX      #FIGFE1
E388  PD E7 CD              JSP      OUTSTF
E38P  P6 FP C8  STAPT1  LDA A    PIAORA
E38E  97 00                 STA A    STDYT
E390  86 01                 LDA A    #$01
E392  97 2F                 STA A    HTPIT
E394  PD E7 0P              JSP      CLPFT
E397  CE E2 D1              LDX      #CLEAPI
E39A  PD E7 CD              JSP      OUTSTF
E39D  CE E6 11              LDX      #INTPT
E3A0  FF FF F8              STX      INTVCT
E3A2  0E                    CLI
                         ** DISPLAY ROUTINE
                         ** 1STPFT -- 1ST PUFFEF-FLAG TEST
                          *             -- TESTS EMPTYNESS OF
                          *             -- THE FIRST PUFFEP
 E3A4  7D 00 40  1STPFT  TST       BUF1FT
```

```
E3A7  26 24                   BNE     ISBFFL
                   **         SNDBFT -- '2ND BUFFER-FLAG TEST'
                    *                   -- TEST THE EMPTYNESS OF
                    *                   -- THE SECOND BUFFER
 E3A9  7D 00 41  SNDBFT  TST     BUF2PT
E3AC  26 2C                   BNE     SDBFFL
                   **         THDBFT -- '3RD BUFFER-FLAG TEST'
                   *                   -- TESTS THE EMPTYNESS OF
                   *                   -- THE THIRD BUFFER
 E3AF  7D 00 42  THDBFT  TST     BUF3PT
E3B1  26 34                   BNE     TDBFFL
                   **         FTHBFT -- '4TH BUFFER-FLAG TEST'
                    *                   -- TESTS THE EMPTYNESS OF
                   *                   -- THE FOURTH BUFFER
 E3B3  7D 00 43  FTHBFT  TST     BUF4PT
E3B6  26 3C                   BNE     FTBFFL
                   **         FFHBFT -- '5TH BUFFER-FLAG TEST'
                   *                   -- TESTS THE EMPTYNESS OF
                    *                   -- THE FIFTH BUFFER
 E3B8  7D 00 44  FFHBFT  TST     BUF5PT
E3BB  26 FB                   BNE     FFHBFT
E3BD  3E                      WAI
E3BE  20 E4                   BRA     ISTBFT
                   **         FFHBFL -- '5TH BUFFER FULL'
 E3C0  CE 00 5F  FFHBFL  LDX     #FFHBUF
E3C3  DF 36                   STX     BFLIND
E3C5  BD F4 01                JSR     BFDSPT
E3C8  7F 00 44                CLR     BUF5PT
E3CB  20 D7                   BRA     ISTBFT
                   **         ISBFFL --'1ST BUFFER FULL'
 E3CD  CE 00 47  ISBFFL  LDX     #ISTBUF
E3D0  DF 36                   STX     BFLIND
E3D2  BD F4 01                JSR     BFDSPT
E3D5  7F 00 40                CLR     BUF1PT
E3D8  20 CF                   BRA     SNDBFT
                   **         SDBFFL -- '2ND BUFFER FULL'
 E3DA  CE 00 4D  SDBFFL  LDX     #SNDBUF
E3DD  DF 36                   STX     BFLIND
E3DF  BD F4 01                JSR     BFDSPT
E3E2  7F 00 41                CLR     BUF2PT
E3E5  20 C8                   BRA     THDBFT
                   **         TDBFFL -- '3RD BUFFER FULL'
 E3E7  CE 00 53  TDBFFL  LDX     #THDBUF
E3EA  DF 36                   STX     BFLIND
E3EC  BD F4 01                JSR     BFDSPT
E3EF  7F 00 42                CLR     BUF3PT
E3F2  20 BF                   BRA     FTHBFT
                   **         FTBFFL -- '4TH BUFFER FULL'
 E3F4  CE 00 59  FTBFFL  LDX     #FRTBUF
E3F7  DF 36                   STX     BFLIND
E3F9  BD F4 01                JSR     BFDSPT
E3FC  7F 00 43                CLR     BUF4PT
E3FF  20 B7                   BRA     FFHBFT
                   **         BFDSPT -- 'BUFFER DISPLAY ROUTINE'
                    *                   -- DISPLAYS THE CONTENTS OF
```

```
F403  81 01             CMP A   #$01
F405  27 1A             PEQ     FFFTPN
F407  81 02             CMP A   #$02
F409  27 20             BEQ     FFSTPN
F40B  81 03             CMP A   #$03
F40D  27 26             PEQ     THIDTPN
F40F  81 04             CMP A   #$04
F411  27 2C             PEQ     FPTTPN
F413  81 05             CMP A   #$05
F415  27 32             PEQ     SFFTPN
F417  CE F1 14          LIX     #CUPS22
F41A  PD F7 CD          JSP     OUTSTP
F41D  PD F4 53          JSP     DSPLAY
F420  39                PTS
                **      FFFTPN -- '1ST FIGUPE FIPST TPANSDUCEP'
 F421  CE F1 8F   FFFTPN  LIX     #CUPS11
F424  PD F7 CD          JSP     OUTSTP
F427  PD F4 53          JSP     DSPLAY
F42A  39                PTS
                **      FFSTPN -- '1ST FIGUPE SECOND TPANDUCEP'
 F42B  CE F1 9D   FFSTPN  LIX     #CUPS12
F42E  PD F7 CD          JSP     OUTSTP
F431  PD F4 53          JSP     DSPLAY
F434  39                PTS
                **      THIDTPN -- 'THIPD TPANSDUCEP'
 F435  CE F1 AP   THIDTPN  LIX     #CUPS13
F438  PD F7 CD          JSP     OUTSTP
F43B  PD F4 53          JSP     DSPLAY
F43E  39                PTS
                **      FPTTPN -- '4TH TPANDSDUCEP'
 F43F  CE F1 B9   FPTTPN  LIX     #CUPS14
F442  PD F7 CD          JSP     OUTSTP
F445  PD F4 53          JSP     DSPLAY
F448  39                PTS
                **      SFFTPN -- '2ND FIGUPE FIPST TRANSDUCEP'
 F449  CE F1 C6   SFFTPN  LIX     #CUPS21
F44C  PD F7 CD          JSP     OUTSTP
F44F  PD F4 53          JSP     DSPLAY
F452  39                PTS
                **      DSPLAY -- 'DISPLAY'
                *              -- DISPLAYS THE CONTENTS
                 *              -- THE BUFFEP CHOSEN
 F453  DE 36      DSPLAY  LDX     BFLINI
F455  A6 01             LDA A   1,X
F457  E6 02             LDA B   2,X
F459  46                POP A
F45A  56                POP B
F45B  PD F6 43          JSP     CVBTD
F45E  CE F1 E1          LDX     #BLANK
F461  PD F7 CD          JSP     OUTSTP
F464  DE 36             LDX     BFLINI
F466  A6 03             LDA A   3,X
F468  E6 04             LDA B   4,X
F46A  46                POP A
F46B  56                POP B
```

```
F46C  BD E6 43          JSR     CVBTD
F46F  DE 26             LDX     BFLIND
F471  A6 05             LDA A   5,X
F473  4D                TST A
F474  26 07             BNE     LCLRRT
F476  CE E3 0A          LDX     #ENGAGD
F479  BD E7 CD          JSR     OUTSTR
F47C  39                RTS
F47D  B6 FB CA  LCLRRT  LDA A   PIAORB
F480  85 80             BIT A   #$80
F482  27 08             BEQ     LCLRT1
F484  CE E2 5B          LDX     #CLROR2
F487  BD E7 CD          JSR     OUTSTR
F48A  20 06             BRA     CLEAR
F48C  CE E1 FC  LCLRT1  LDX     #CLROR1
F48F  BD E7 CD          JSR     OUTSTR
F492  CE E2 D1  CLEAR   LDX     #CLEARD
F495  BD E7 CD          JSR     OUTSTR
F498  BD E7 0D          JSR     CLRRT
F49B  39                RTS
F49C  B6 FB C8  START   LDA A   PIAORA
F49F  98 00             EOR A   STBYT
F4A1  CE F0 00          LDX     #INIDX1
F4A4  C6 01     TIRT    LDA B   #$01
F4A6  F7 FB CA          STA B   PIAORB
F4A9  C6 08             LDA B   #$08
F4AB  D7 01             STA B   CNT1
F4AD  0C        LOOP2   CLC
F4AE  46                ROR A
F4AF  97 30             STA A   STOREA
F4B1  25 46             BCS     SUBRT1
F4B3  7A 00 01  LOOP3   DEC     CNT1
F4B6  7D 00 01          TST     CNT1
F4B9  26 F2             BNE     LOOP2
F4BB  B6 FB C8          LDA A   PIAORA
F4BE  B1 E2 D0          CMP A   CLRBYT
F4C1  26 2C             BNE     ENGRT
F4C3  96 04             LDA A   IN1
F4C5  91 08             CMP A   OUT1
F4C7  26 26             BNE     ENGRT
F4C9  96 03             LDA A   IN11
F4CB  91 07             CMP A   OUT11
F4CD  26 20             BNE     ENGRT
F4CF  96 06             LDA A   IN2
F4D1  91 0A             CMP A   OUT2
F4D3  26 1A             BNE     ENGRT
F4D5  96 05             LDA A   IN22
F4D7  91 09             CMP A   OUT22
F4D9  26 14             BNE     ENGRT
F4DB  86 02             LDA A   #$02
F4DD  B7 FB CA          STA A   PIAORB
F4E0  DE 45             LDX     BUFIND
F4E2  C6 01             LDA B   #$01
F4E4  E7 05             STA B   5,X
F4E6  3B                RTI
```

```
F4E9  B7 FB CA                STA A   PIAORB
F4EC  7E F6 02                JMP     SUSPND
                        **    ENGRT -- 'ENGAGED ROUTINE'
                         *          -- GIVES THE INDICATION
F4EF  86 01          ENGRT    LDA A   #$01
F4F1  B7 FB CA                STA A   PIAORB
F4F4  DE 4E                   LDX     BUFIND
F4F6  6F 05                   CLR     5,X
F4F8  3B                      RTI
F4F9  D6 01          SUBRT1   LDA B   CNT1
F4FB  C1 04                   CMP B   #$04
F4FD  2E 0F                   BGT     SUBRT3
F4FF  D6 01          SUBRT2   LDA B   CNT1
F501  D7 02                   STA B   CNT2
F503  CB 04                   ADD B   #$04
F505  D7 01                   STA B   CNT1
F507  BD F5 AF                JSR     RTCNT2
F50A  96 20                   LDA A   STOREA
F50C  20 A5                   BRA     LOOP3
F50E  D6 01          SUBRT3   LDA B   CNT1
F510  C0 04                   SUB B   #$04
F512  D7 02                   STA B   CNT2
F514  8D 04                   BSR     RTCNT1
F516  96 20                   LDA A   STOREA
F518  20 99                   BRA     LOOP3
F51A  8D 5B          RTCNT1   BSR     CHXBT1
F51C  D6 00                   LDA B   STBYT
F51E  E5 00                   BIT B   0,X
F520  27 11                   BEQ     LHTRT1
                        **    HLTRT1 -- 'HIGH TO LOW TRANSITION ONE'
F522  E6 00          HLTRT1   LDA B   0,X
F524  53                      COM B           UPDATING THE STATUSBYTE
F525  D4 00                   AND B   STBYT
F527  D7 00                   STA B   STBYT
F529  8D 5A                   BSR     CHXBT2
F52B  D6 00                   LDA B   STBYT
F52D  E5 00                   BIT B   0,X
F52F  27 62                   BEQ     OUTICT  OUTICOUNT
F531  20 12                   BRA     INICNT  INICOUNT
                        **    LHTRT1 -- 'LOW TO HIGH TRANSTION ONE'
F533  E6 00          LHTRT1   LDA B   0,X
F535  DA 00                   ORA B   STBYT   UPDATING THE STATUSBYTE
F537  D7 00                   STA B   STBYT
F539  8D 4A                   BSR     CHXBT2
F53B  D6 00                   LDA B   STBYT
F53D  E5 00                   BIT B   0,X
F53F  26 52                   BNE     OUTICT
F541  20 02                   BRA     INICNT
F543  20 A8          FLRT2    BRA     FLRT
                        **    INICNT -- 'INICOUNT'
                        *            -- INCREMENTS THE GLOBAL AND
                         *           -- LOCAL INICOUNTS
F545  D6 04          INICNT   LDA B   INI
F547  5D                      TST B
```

```
FF48   26 1B                      BNE      NECT1
FF4A   37                         PSH B
FF4B   C6 80                      LDA B    #$80
FF4D   F5 FB CA                   BIT B    FIAORB
FF50   27 05                      BEQ      ONEHD
FF52   CE F0 42                   LDX      #HTBT+1
FF55   20 03                      BRA      FILF
FF57   CE F0 41       ONEHD       LDX      #HTBT
FF5A   E6 00          FILF        LDA B    0,X
FF5C   F5 FB C8                   BIT B    FIAORA
FF5F   26 03                      BNE      NECT
FF61   7F 00 2F                   CLR      HTBIT
FF64   33             NECT        PUL B
FF65   5C             NECT1       INC B
FF66   D7 04                      STA B    IN1
FF68   D6 03                      LDA B    IN11
FF6A   C9 00                      ADC B    #$00
FF6C   D7 03                      STA B    IN11
FF6E   BD E6 77                   JSR      LCLCT1
FF71   BD E6 8A                   JSR      LINICT
FF74   39                         RTS
FF75   20 CC          FLRT4       BRA      FLRT2
FF77   CE F0 00       CHXRT1      LDX      #INDEX1
FF7A   DF 2B                      STX      CHBYT1
FF7C   D6 2C                      LDA B    CHBYT2
FF7E   DB 01                      ADD B    CNT1
FF80   D7 2C                      STA B    CHBYT2
FF82   DE 2B                      LDX      CHBYT1
FF84   39                         RTS
FF85   CE F0 00       CHXRT2      LDX      #INDEX1
FF88   DF 2D                      STX      CHBYT3
FF8A   D6 2E                      LDA B    CHBYT4
FF8C   DB 02                      ADD B    CNT2
FF8E   D7 2E                      STA B    CHBYT4
FF90   DE 2D                      LDX      CHBYT3
FF92   39                         RTS
                      **          OUTICT -- 'OUTICOUNT'
                      *                  -- INCREMENTS GLOBAL AND
                       *                   -- LOCAL OUTICOUNT
FF93   7D 00 04       OUTICT      TST      IN1
FF96   27 AB                      BEQ      FLRT2
FF98   D6 08                      LDA B    OUT1
FF9A   5C                         INC B
FF9B   D7 08                      STA B    OUT1
FF9D   D6 07                      LDA B    OUT11
FF9F   C9 00                      ADC B    #$00
FFA1   D7 07                      STA B    OUT11
FFA3   BD E6 77                   JSR      LCLCT1
FFA6   BD E6 9C                   JSR      LOUTIT
FFA9   BD E6 B5                   JSR      ORIGIN
FFAC   39                         RTS
FFAD   20 C6          FLRT3       BRA      FLRT4
FFAF   8D D4          RTCNT2      BSR      CHXRT2
FFB1   D6 00                      LDA B    STBYT
```

```
F5B9  53                    COM B   UPDATING THE STATUSBYTE
F5BA  D4 00                 AND B   STBYT
F5BC  D7 00                 STA B   STBYT
F5BE  8D B7                 BSR     CHXBT1
F5C0  D6 00                 LDA B   STBYT
F5C2  E5 00                 BIT B   0,X
F5C4  27 10                 BEQ     IN2CNT
F5C6  20 23                 BRA     OUT2CT
F5C8  E6 00        LHTBT2   LDA B   0,X
F5CA  DA 00                 ORA B   STBYT    UPDATING THE STATUSBYTE
F5CC  D7 00                 STA B   STBYT
F5CE  8D A7                 BSR     CHXBT1
F5D0  D6 00                 LDA B   STBYT
F5D2  E5 00                 BIT B   0,X
F5D4  27 15                 BEQ     OUT2CT
                   **       IN2CNT -- 'IN1COUNT'
                   *                -- INCREMENTS GLOBAL AND
                   *                -- LOCAL IN1COUNTS
F5D6  D6 06        IN2CNT   LDA B   IN2
F5D8  5C                    INC B
F5D9  D7 06                 STA B   IN2
F5DB  D6 05                 LDA B   IN22
F5DD  C9 00                 ADC B   #$00
F5DF  D7 05                 STA B   IN22
F5E1  BD F6 77              JSR     LCLCT1
F5E4  BD E6 90              JSR     LIN2CT
F5E7  BD F6 B5              JSR     ORIGIN
F5EA  39                    RTS
                   **       OUT2CT -- 'OUT2COUNT'
                   *                -- INCREMENTS GLOBAL AND
                   *                -- LOCAL OUT2COUNTS
F5EB  7D 00 04     OUT2CT   TST     IN1
F5EE  27 BD                 BEQ     FLPT3
F5F0  D6 0A                 LDA B   OUT2
F5F2  5C                    INC B
F5F3  D7 0A                 STA B   OUT2
F5F5  D6 09                 LDA B   OUT22
F5F7  C9 00                 ADC B   #$00
F5F9  D7 09                 STA B   OUT22
F5FB  BD E6 77              JSR     LCLCT1
F5FE  BD F6 A3              JSR     LOUT2T
F601  39                    RTS
F602  CE F0 13     SUSPND   LDX     #NEG1
F605  BD E7 CD              JSR     OUTSTR
F608  CE F0 19              LDX     #FAULT
F60B  BD E7 CD              JSR     OUTSTR
F60E  01           LP       NOP
F60F  20 FD                 BRA     LP
                   **       INTRT -- 'INTERRUPT ROUTINE'
F611  86 80        INTRT    LDA A   #$80
F613  B5 FB C9              BIT A   PIACRA
F616  26 1D                 BNE     START2
F618  B5 FB CB              BIT A   PIACRB
F61B  26 03                 BNE     HALTRT
F61D  BD F4 E7              JSR     FLPT
```

```
F620  7D 00 2F  HALTPT  TST     HTBIT
F623  27 13             BEQ     INHOT
F625  96 07     OUTHOT  LDA A   OUT11
F627  D6 08             LDA B   OUT1
F629  CB 02             ADD B   #$02
F62B  89 00             ADC A   #$00
F62D  0C                CLC
F62E  46                ROR A
F62F  56                ROR B
F630  BD F6 43          JSR     CVBTD
F633  0E                CLI
F634  3B                RTI
F635  7E F4 9C  START2  JMP     START
F638  96 03     INHOT   LDA A   IN11
F63A  D6 04             LDA B   IN1
F63C  0C                CLC
F63D  46                ROR A
F63E  56                ROR B
F63F  BD F6 43          JSR     CVBTD
F642  3B                RTI
                **      CVBTD -- 'CONVERSION OF BINARY TO
                *                              DECIMAL'
F643  CE F6 6D  CVBTD   LDX     #K10K
F646  7F 00 33  CVDEC1  CLR     SAVEA
F649  E0 01     CVDEC2  SUB B   1,X
F64B  A2 00             SBC A   0,X
F64D  25 05             BCS     CVDEC5
F64F  7C 00 33          INC     SAVEA
F652  20 F5             BRA     CVDEC2
F654  EB 01     CVDEC5  ADD B   1,X
F656  A9 00             ADC A   0,X
F658  36                PSH A
F659  DF 34             STX     SAVEX1
F65B  96 33             LDA A   SAVEA
F65D  8B 30             ADD A   #$30          MAKE ASCII CHAR
F65F  BD F7 A8          JSR     OUTCH
F662  32                PUL A                 RESTORE A
F663  DE 34             LDX     SAVEX1
F665  08                INX
F666  08                INX
F667  8C F6 77          CPX     #K10K+10
F66A  26 DA             BNE     CVDEC1
F66C  39                RTS
                *       CONSTANTS FOR CONVERSION
F66D  27 10     K10K    FDB     10000
F66F  03 E8             FDB     1000
F671  00 64             FDB     100
F673  00 0A             FDB     10
F675  00 01             FDB     1
F677  CE E0 09  LCLCT1  LDX     #INDEX
F67A  D6 02             LDA B   CNT2
F67C  08        LOOP    INX
F67D  08                INX
F67E  5A                DEC B
F67F  26 FB             BNE     LOOP
```

```
 F684  E6 01     LINICT  LDA B   1,X
 F686  5C                INC B
 F687  E7 01             STA B   1,X
 F689  E6 00             LDA B   0,X
 F68B  C9 00             ADC B   #$00
 F68D  E7 00             STA B   0,X
 F68F  39                RTS
                 **      LIN2CT -- 'LOCAL IN2COUNT'
                 *              -- INCREMENTS LOCAL IN2COUNT
 F690  E6 03     LIN2CT  LDA B   3,X
 F692  5C                INC B
 F693  E7 03             STA B   3,X
 F695  E6 02             LDA B   2,X
 F697  C9 00             ADC B   #$00
 F699  E7 02             STA B   2,X
 F69B  39                RTS
                 **      LOUTIT -- 'LOCAL OUTICOUNT'
                 *              -- INCREMENTS LOCAL OUTICOUNT
 F69C  E6 05     LOUTIT  LDA B   5,X
 F69E  5C                INC B
 F69F  E7 05             STA B   5,X
 F6A1  E6 04             LDA B   4,X
 F6A3  C9 00             ADC B   #$00
 F6A5  E7 04             STA B   4,X
 F6A7  39                RTS
                 **      LOUT2T -- 'LOCAL OUT2COUNT'
                 *              -- INCREMENTS LOCAL OUT2COUNT
 F6A8  E6 07     LOUT2T  LDA B   7,X
 F6AA  5C                INC B
 F6AB  E7 07             STA B   7,X
 F6AD  E6 06             LDA B   6,X
 F6AF  C9 00             ADC B   #$00
 F6B1  E7 06             STA B   6,X
 F6B3  39                RTS
 F6B4  DF 21     ORIGIN  STX     INDEX2
 F6B6  96 02             LDA A   CNT2
 F6B8  81 04             CMP A   #$04
 F6BA  27 23             BEQ     ISTTR
 F6BC  81 03             CMP A   #$03
 F6BE  27 06             BEQ     STTR
 F6C0  81 02             CMP A   #$02
 F6C2  27 3D             BEQ     TDTTR
 F6C4  20 32             BRA     FDTTR
 F6C6  C6 80     STTR    LDA B   #$80
 F6C8  F5 FB CA          BIT B   PIAORB
 F6CB  27 09             BEQ     FSFG2
 F6CD  BD F7 21          JSR     SEARCH
 F6D0  86 06             LDA A   #$06
 F6D2  BD F7 7E          JSR     BFLOAD
 F6D5  39                RTS
 F6D6  BD F7 21  FSFG2   JSR     SEARCH
 F6D9  86 02             LDA A   #$02
 F6DB  BD F7 7E          JSR     BFLOAD
```

```
F6DE   39                     RTS
F6DF   C6 80       ISTTR      LDA B   #$80
F6E1   F5 FD CA               BIT B   FIAORB
F6E4   27 09                  BEQ     FSRG1
F6E6   BD F7 21               JSR     SEARCH
F6E9   86 05                  LDA A   #$05
F6EB   BD F7 7D               JSR     BFLOAD
F6EE   39                     RTS
F6EF   BD F7 21    FSRG1      JSR     SEARCH
F6F2   86 01                  LDA A   #$01
F6F4   BD F7 7D               JSR     BFLOAD
F6F7   39                     RTS
F6F8   BD F7 21    FITTR      JSR     SEARCH
F6FB   86 04                  LDA A   #$04
F6FD   BD F7 7D               JSR     BFLOAD
F700   39                     RTS
F701   BD F7 21    TITTR      JSR     SEARCH
F704   86 03                  LDA A   #$03
F706   BD F7 7D               JSR     BFLOAD
F709   39                     RTS
F70A   CE 00 03    CLRPT      LDX     #CLRIND
F70D   6F 00       CLRPT1     CLR     0,X
F70F   08                     INX
F710   8C 00 2B               CPX     #CLRBII+1
F713   26 F8                  BNE     CLRPT1
                   **         BUFCLR -- 'BUFFER CLEAR'
                    *                 -- CLEARS THE BUFFERS
F715   CE 00 40    BUFCLR     LDX     #BUF1PT
F718   6F 00       BFCLR1     CLR     0,X
F71A   08                     INX
F71B   8C 00 65               CPX     #BUFEND+1
F71E   26 F8                  BNE     BFCLR1
F720   39                     RTS
                   **         SEARCH -- 'SEARCH'
                   *                 -- SEARCHES EMPTY BUFFER
                    *                       FOR LOADING IT
F721   7D 00 44    SEARCH     TST     BUF5PT
F724   26 41                  BNE     SERCH2
F726   7D 00 43               TST     BUF4PT
F729   26 32                  BNE     LD5BUF
F72B   7D 00 42               TST     BUF3PT
F72E   26 25                  BNE     LD4BUF
F730   7D 00 41               TST     BUF2PT
F733   26 17                  BNE     LD3BUF
F735   7D 00 40               TST     BUF1PT
F738   26 09                  BNE     LD2BUF
                   **         LD1BUF -- 'LOAD THE FIRST BUFFER'
F73A   CE 00 47    LD1BUF     LDX     #1STBUF
F73D   DF 45                  STX     BUFIND
F73F   7C 00 40               INC     BUF1PT
F742   39                     RTS
                   **         LD2BUF -- 'LOAD THE SECOND BUFFER'
F743   CE 00 4D    LD2BUF     LDX     #SNDBUF
F746   DF 45                  STX     BUFIND
F748   7C 00 41               INC     BUF2PT
```

```
 F74C  CE 00 53  LD3BUF  LDX      #THDBUF
F74F  DF 45              STX      BUFIND
F751  7C 00 42           INC      BUF3PT
F754  39                 RTS
               **        LD4BUF --  'LOAD THE FOURTH BUFFER'
 F755  CE 00 59  LD4BUF  LDX      #FRTBUF
F758  DF 45              STX      BUFIND
F75A  7C 00 43           INC      BUF4PT
F75D  39                 RTS
               **        LD5BUF --  'LOAD THE FIFTH BUFFER'
 F75E  CE 00 5F  LD5BUF  LDX      #FFHBUF
F761  DF 45              STX      BUFIND
F763  7C 00 44           INC      BUF5PT
F766  39                 RTS
F767  7D 00 40  SERCH2   TST      BUF1PT
F76A  27 CE              BEQ      LD1BUF
F76C  7D 00 41           TST      BUF2PT
F76F  27 D2              BEQ      LD2BUF
F771  7D 00 42           TST      BUF3PT
F774  27 16              BEQ      LD3BUF
F776  7D 00 43           TST      BUF4PT
F779  27 1A              BEQ      LD4BUF
F77B  7E F7 99           JMP      BFFALT
               **        BFLOAD --  'BUFFER LOAD'
                *                   -- LOADS THE BUFFER FOR DISPLAY
 F77E  A7 00      BFLOAD  STA A    0,X
F780  DE 21              LDX      INDEX2
F782  A6 02              LDA A    2,X
F784  E6 03              LDA B    3,X
F786  DE 45              LDX      BUFIND
F788  A7 01              STA A    1,X
F78A  E7 02              STA B    2,X
F78C  DE 21              LDX      INDEX2
F78E  A6 04              LDA A    4,X
F790  E6 05              LDA B    5,X
F792  DE 45              LDX      BUFIND
F794  A7 03              STA A    3,X
F796  E7 04              STA B    4,X
F798  39                 RTS
F799  CE F3 48  BFFALT   LDX      #BUFFLT
F79C  BD E7 CC           JSR      OUTSTR
F79F  7E F4 E7           JMP      FLRT
               **        OUT4HS  -- OUPUT FOUR HEX DIGITS AND
                 *          ENTRY:  <X> - ADDRESS OF BYTES
                *          EXIT :   X    INCREMENTED PAST BYTES
                 *          USES:     A,X
F7A2  8D 11     OUT4HS   BSR      THB
               **        OUT2HS  --  OUTPUT TWO HEX DIGITS AND
                 *                        ENTRY,EXIT,USES -- SEE
 F7A4  8D 0F      OUT2HS  BSR      THB
               **        OUTSP  --  OUTPUT SPACE CODE
                 *                        ENTRY :NONE:EXIT: <A> =
 F7A6  86 20      OUTSP   LDA A   #' '
                *        OUTCH -- OUTPUT CHARACTYEEEER TO CONSOLE
                 *          ENTRY -- <A> = ASCII VALUE OF CHARACTR
```

```
F7A8  37          OUTCH    PSH B
F7A9  C6 02                LDA B   #2
F7AB  F5 FB CD    OUTT1    BIT B   ACIAST
F7AE  27 FB                BEQ     OUTT1
F7B0  B7 FB CF             STA A   ACIADT
F7B3  33                   PUL B
F7B4  39          OUTT2    RTS
                  *        THB  -- TYPE HEX BYTES
                  *        ENTRY : -X> - ADDRESS OF BYTE TO OUTPUT
                  *         EXIT  : -X> - OLDVALUE+1
                  *         USES  : A  ,C
F7B5  A6 00       THB      LDA A     0,X
F7B7  08                   INX
                  *        THB0  -- TYPE -A> IN HEX
                  *         ENTRY : -A> - VALUE
                  *        EXIT  : VALUE TYPED
F7B8  36          THB0     PSH A
F7B9  44                   LSR A
F7BA  44                   LSR A
F7BB  44                   LSR A
F7BC  44                   LSR A
F7BD  8D 02                BSR THB1
F7BF  32                   PUL A
F7C0  84 0F                AND A   #$F
F7C2  81 0A       THB1     CMP A   #10
F7C4  25 02                BCS     THB2
F7C6  8B 07                ADD A   #7
F7C8  8B 30       THB2     ADD A   #$30
F7CA  20 DC       OUTCHB   BRA     OUTCH
                  **       OUTSTR  -- OUTPUT CHARACTER STRING TO C
                    *        ENTRY    -- -X> = ADDRESS OF STRING
                    *        EXIT     -- -X> = INCREMENTED PAST END
                    *                            END OF STRING MARKER
                    *        USES     --               A,X,C
F7CC  A6 00       OUTSTR   LDA A    0,X
F7CE  08                   INX
F7CF  8D F9       OUTST2   BSR     OUTCHB
F7D1  2A F9                BPL     OUTSTR
F7D3  39          OUTST3   RTS
F7D4                       END
```

STATEMENTS =826

FREE BYTES =11158

NO ERRORS DETECTED